DEC STD 052-4 Local Direct Connection (no Modem) for Serial Asynchronous Terminals and System Interfaces

DOCUMENT IDENTIFIER: A-DS-EL00052-04-0000 Rev C, 01-Jul-1990

ABSTRACT: This standard defines minimum electrical interface requirements for direct connections drivers and receivers, specifies required protections from Electrical OverStress (EOS) and ElectroStatic Discharge (ESD), and defines the connectors/cables used for direct, asynchronous, serial connection between data terminal equipment (DTE). This standard is intended for use at data signaling rates up to 40,000 bits per second and provides a summary of the known data on the use of this standard at distances up to 4000 feet (1200 meters).

APPLICABILITY: This standard is mandatory for all new hardware designs for terminals, terminal servers, personal computers, workstations, small-packaged computers, and communications options. Nonconformance with this standard must be approved by the Telecommunications Domain Manager.

STATUS: APPROVED 01-Jul-1990; use VTX SMC for current status.

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1 INTRODUCTION

1.1 PURPOSE

This standard describes the electrical property requirements for direct connection interfaces to support direct, asynchronous, serial connection between Digital's data terminal equipment (DTE) products. All new products shall use this standard for local direct connection. If a modem connection is required, an EIA 232-D port shall be configured, using DEC423 drivers and receivers and associated protection devices, that complies with *DEC STD 052-2 Electrical Requirements for Binary Interfaces that Conform to EIA 232-D or CCITT V.28.*

DEC423 was chosen because it is interoperable with EIA 232D *Interface Between Data Terminal Equipment and Data Communication Equipment Employing Serial Binary Data Interchange*, EIA 423, EIA 422, EIA 485 *Electrical Characteristics of Generators and Receivers for use in Balanced Digital Multi Point Systems*, EIA 530, DEC232, DEC423-A *Electrical Characteristics of Unbalanced Voltage Digital Interface Circuits*, DEC422-A/*Electrical Characteristics of Balanced Voltage Digital Interface Circuits*, CCITT V.28 *Electrical Characteristics for V.28 Unbalanced Double-Current Interchange Circuits*, CCITT V.10, and CCITT V.11. Because of its interoperability with all the standards, this places requirements on the components used that surpass industry standards.

NOTE

As of December 1985, the Electronic Industries Association (EIA) conforms to international standards. The "RS-" identifier is replaced with "EIA-". Therefore, RS-232-C is replaced by EIA 232-D, RS-423-A is replaced by EIA 423-A, and RS-422-A is replaced by EIA 422-A.

1.2 SCOPE

This standard applies to the drivers, receivers, protection devices, and connectors/cables used for "local direct connection". A local direct connection is an electrical connection made between DTEs without using modems, limited distance adapters, switches, or long line drivers. This standard must be met for point-to-point, full-duplex, serial, asynchronous terminal and computer interfaces whose design begins after the approval date of this standard. DEC423 meets all the requirements of EIA 423-A/CCITT V.10 *Electrical Characteristics for V.10 Unbalanced Double-Current Interchange Circuits for General Use with Integrated Circuit Equipment in the Field of Data Communications*, but has placed more stringent requirements on generator and load characteristics so that DEC423 drivers and receivers comply with EIA 232-D and CCITT V.28 requirements, and provide improved speed/distance performance and noise immunity.

DEC422 meets all the requirements of EIA 422-A/CCITT V.11, but has placed more stringent requirements on generator and load characteristics so that DEC422 drivers can be protected, drive longer distances. DEC422 is shown here to document its interoperability with DEC423. Note that DEC423 receivers are providing improved speed/distance performance, cross compatibility and noise immunity.

This standard shall not restrict other serial line connection schemes in markets and environments other than the usual office and business settings. For example, serial line connections on the factory floor, to laboratory equipment, to Tempest devices, and to medical devices in patient care areas may require methods of connection beyond the scope of this standard.

This standard does not apply to NEMA type 3, 3R, 4, 4X, 9, 12, and 13 environments, UL 544 environments, or to hazardous environments.

If a market or environment is deemed to require methods of connection beyond the scope of this standard, the Design Engineer shall request that conformance to this standard be waived according to the guidelines cited in *DEC STD 066-2 Waivers to Digital Design Standards.*

1.3 NON-GOALS

This standard states the minimum requirements for meeting DEC423 and is not intended to be a design guide. For a more detailed discussion of the implementation of this standard, refer to *Design Guidelines for Serial Asynchronous Interfaces [EK-EIADS-HM-001].* Updated versions are available from Ralph Dieter, ENET: WORDS::DIETER.

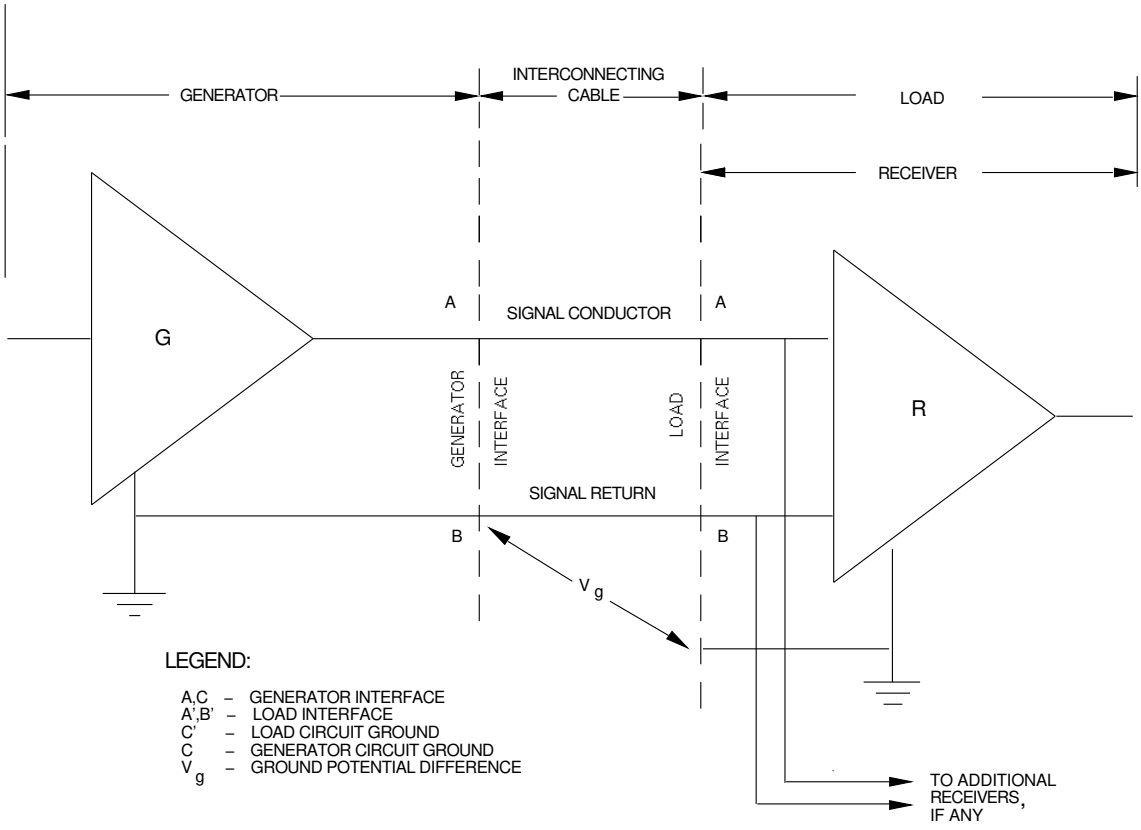
This standard does not address building (facility) wiring rules and conventions.

2 ELECTRICAL CHARACTERISTICS

The balanced and unbalanced voltage digital interface circuit, is shown in Figure 1. The circuit consists of the following parts: The generator (G), the interconnecting cable, and the load. The load is comprised of one or more receivers (R).

The electrical characteristics of the generator and receiver are specified in terms of direct electrical measurements, while the interconnecting cable is described in terms of its electrical and physical characteristics.

Figure 1: Unbalanced Digital Interface Circuit



2.1 DEC423 GENERATOR CHARACTERISTICS

The electrical characteristics of a generator, including waveshaping provisions, are specified in terms of the measurements illustrated in Figures 2 and 3. A generator circuit meeting these requirements results in a low impedance (50 ohms or less) unbalanced voltage source that will supply a voltage to the interconnecting cable in the range of 5 volts to 6 volts. The signaling sense of the voltages appearing across the interconnecting cable is defined as follows.

- The A terminal of the generator shall be negative with respect to the C terminal for a binary 1 state (Data = 1 = Mark, Control = OFF).
- The A terminal of the generator shall be positive with respect to the C terminal for a binary 0 (data) state (Data=0=space, control=ON).

2.1.1 DEC423 Open Circuit Measurement

The open circuit voltage measurement is taken with a 3900-ohm resistor and protection device connected between points A and C (refer to Figure 2, diagram A). In both binary states, the magnitude of the signal voltage (Vo) shall be equal to or greater than 5.0 volts, but not greater than 6.0 volts.

2.1.2 DEC423 Test Termination Measurement

The test termination is measurement is taken with a test load of 450 ohms, and protection device connected between output points A and C (refer to Figure 2, diagram B). The magnitude of the output voltage (Vt) in both binary states shall be equal to or greater than 0.9 of the magnitude of Vo. Vt- and Vt+ shall be within 0.4 Volts.

2.1.3 DEC423 Short-Circuit Measurement

The short-circuit measurement is taken with output points A and C short-circuited (refer to Figure 2, diagram C). The current (Is) flowing through point A in both binary states shall not exceed 150 milliamperes.

Short-circuit current must be balanced with a minimum short-circuit current of 20 ma. Balance must be within 0.60 to 1.40 mA, both negative and positive short circuit to ground.

Note: Once the cable length exceeds 500 feet, waveform distortion is determined by the short circuit current.

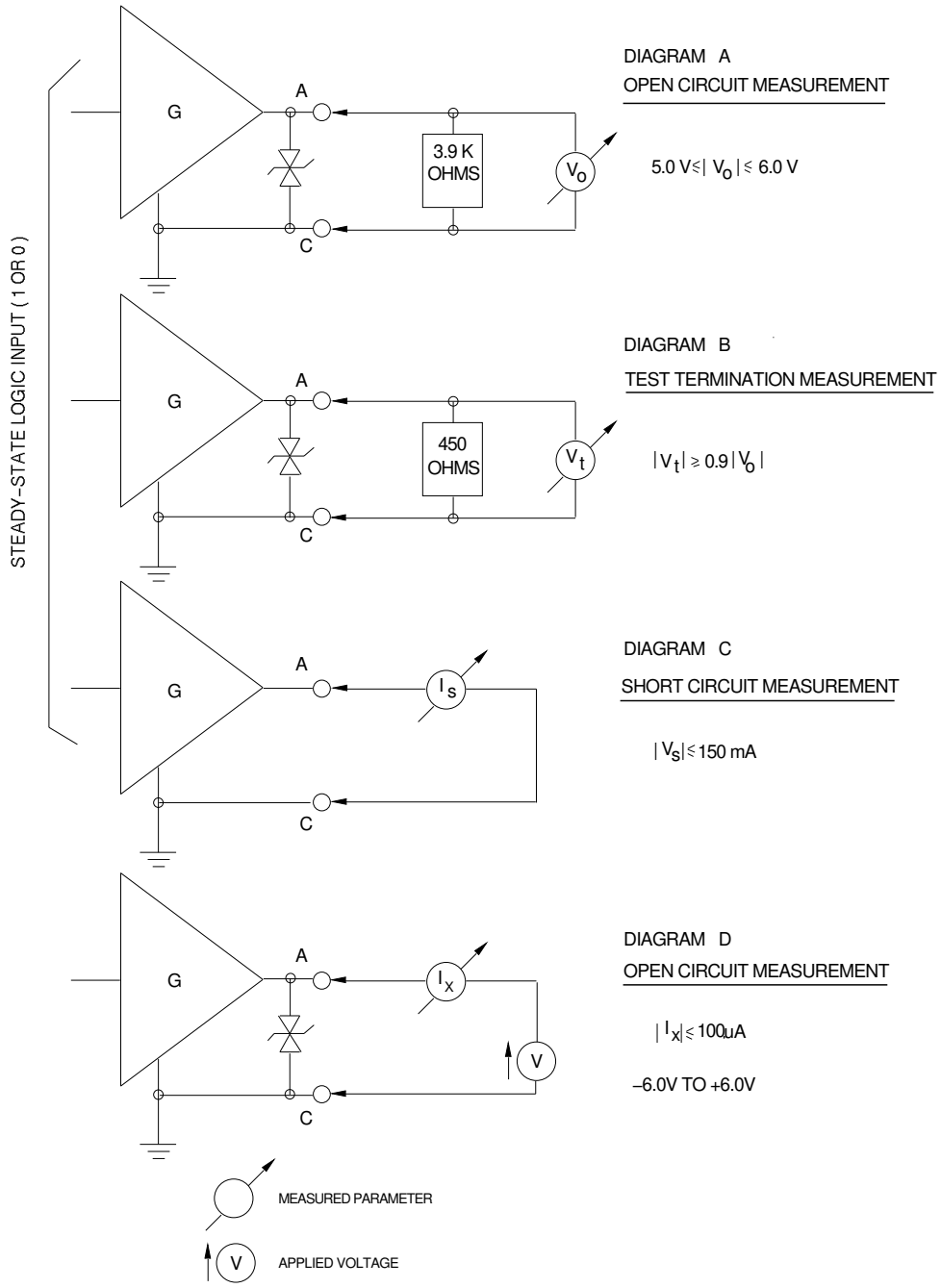
The preferred balanced short circuit current is 40 mA.

2.1.4 DEC423 Power-Off Measurement

The power-off measurement must be taken under power-off conditions, with voltages ranging between +6.0 and -6.0 volts applied between the output point A and point C (refer to Figure 2, diagram D). The magnitude of the generator and protection device output leakage current (Ix) shall not exceed 100 microamperes.

Note: The driver protection circuits guarantee a 35 volt clamp; drivers must not have parasitic latch-up below 35 volts. The 9636 is good only to 16V.

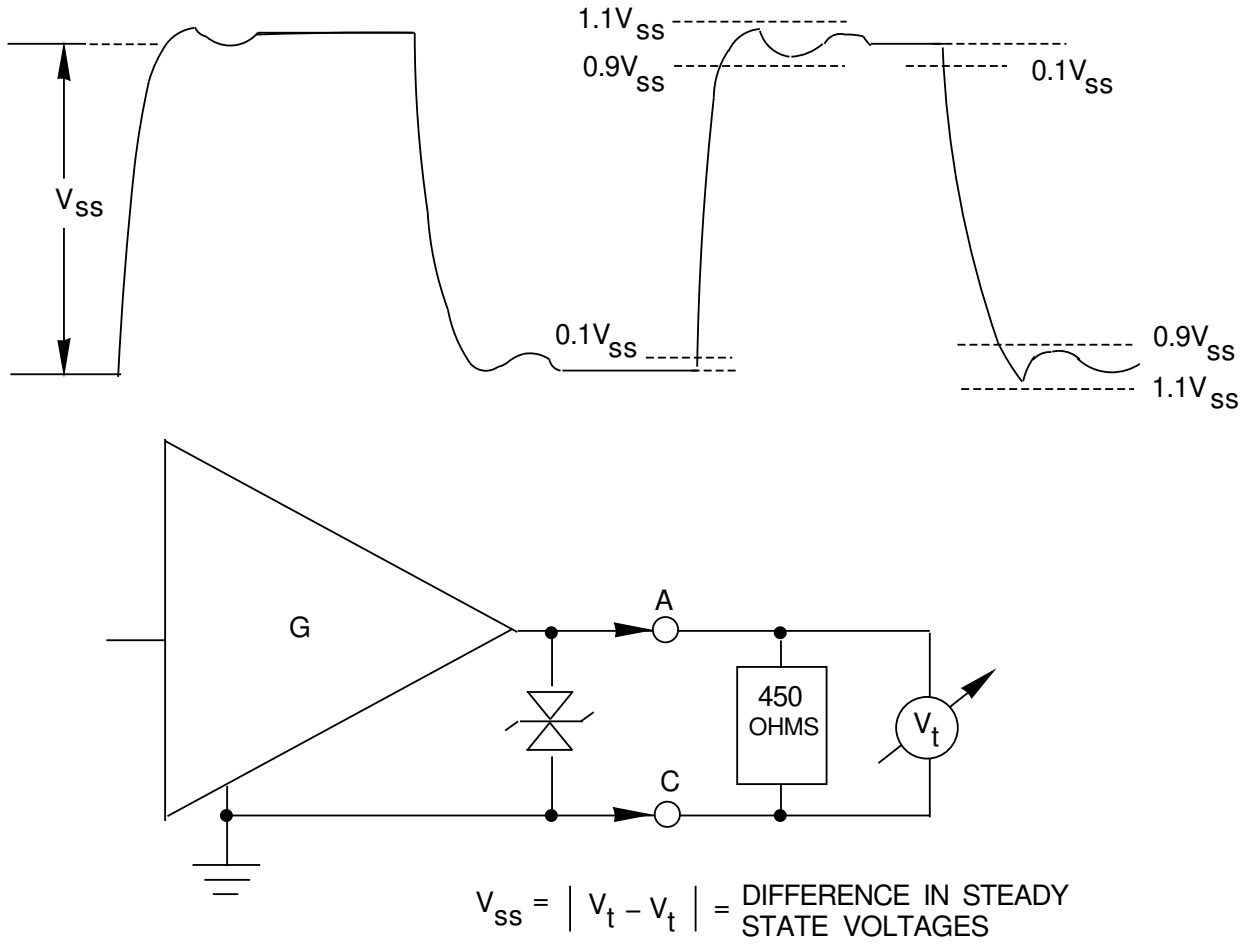
Figure 2: DEC423 - Generator Parameter Measurements



2.1.5 DEC423 Output Signal Waveform

The output signal waveform measurement must be made with a resistor of 450 ohms connected between points A and C (refer to Figure 5). A test signal composed of alternating ones and zeros shall be applied to the input. The change in amplitude of the output signal during transitions from one binary state to the other shall be monotonic between 0.1 and 0.9 of Vss. Thereafter, the signal voltage shall not vary more than 10% of Vss from the steady-state value, until the next binary transition occurs. The instantaneous magnitude of Vt shall neither exceed 6.0 volts, nor be less than 4.5 volts. Vss is defined as the voltage difference between the two steady-state values of the generator output.

Figure 3: Generator Output Signal Wave Form



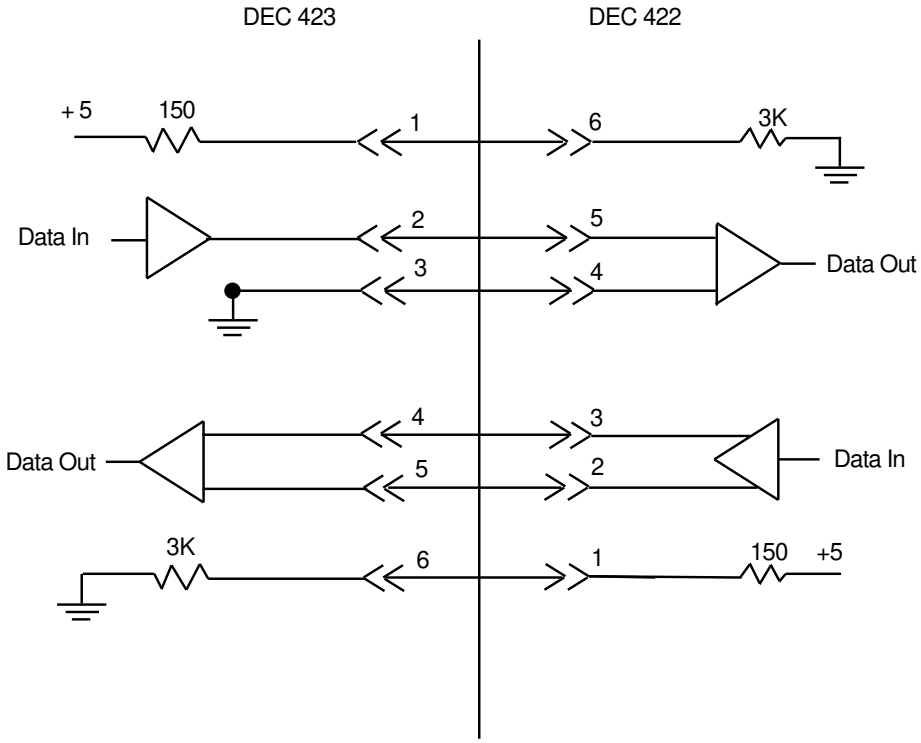
2.1.6 DEC423/EIA 232-D Waveshaping

Waveshaping of the generator output signal shall be used to control the level of interference (near-end crosstalk) that may be coupled to adjacent circuits in an interconnection. The rise time (tr) of the output signal shall be controlled to ensure the signal reaches 0.9 Vss between 0.1 and 0.3 units of the duration of the unit interval (tb) at the maximum data signaling rate to be used.

The recommended rise time range is 3.5 to 7.0 microseconds at the DEC423 maximum data signaling rate of 38.4 kbps.

NOTE: For EIA 232-D, the waveshaping of the generator output signal requires that the time to pass through the transition region (-3 < V < +3) not exceed 0.04 of a bit time. For CCITT V.28, it is 0.03 of a bit time. For DEC423 drivers configured for EIA 232-D/CCITT V.28 running at speeds up to 20 kbps, the recommended rise time range is 1.8 to 2.7 microseconds.

Figure 4: DEC 423 to 422 Interoperation Diagram



2.2 DEC422 GENERATOR CHARACTERISTICS

The electrical characteristics of a generator, including waveshaping provisions, are specified in terms of the measurements illustrated in Figures 4 and 5. A generator circuit meeting these requirements results in a low impedance (50 ohms or less) unbalanced voltage source that will produce a voltage applied to the interconnecting cable in the range of 1.5 volts to 6 volts. The signaling sense of the voltages appearing across the interconnecting cable is defined as follows.

- The A terminal of the generator shall be negative with respect to the B terminal for a binary 1 (MARK or OFF) state.
- The A terminal of the generator shall be positive with respect to the B terminal for a binary 0 (SPACE or ON) state.

2.2.1 DEC422 Open Circuit Measurement

The open circuit voltage measurement is taken with protection devices connected between points A and B (refer to Figure 5, diagram A). In both binary states, the magnitude of the signal voltage (Vo) shall be equal to or greater than 2.0 volts but not greater than 6.0 volts.

2.2.2 DEC422 Test Termination Measurement

The test termination measurement is taken with a test load of 100 ohms, and protection devices connected between output points A and B (termination A) (refer to Figure 5, diagram B). The magnitude of the output voltage (Vt) in both binary states shall be equal to or greater than 2.0 volts with a balance of less than 0.4 volts.

With a test load of 54-ohms (refer to Figure 5, diagram C) and a protection device connected between output points A and B, the magnitude of the output voltage (Vt) in both binary states shall be equal to or greater than 1.5 volts with a balance of less than 0.2 volts.

2.2.3 DEC422 Termination Measurement with Varying Common Mode

The power-off measurement must be taken under power-off conditions, with voltages ranging between +7.0 and -7.0 volts applied between the output point A or B and point C (refer to Figure 5, diagram D).

2.2.4 DEC422 Short-Circuit Measurement

The short-circuit measurement is taken with output points A and B short-circuited (refer to Figure 5, diagram E). The current (Is) flowing through point A or B in both binary states shall not exceed 150 milliamperes.

2.2.5 DEC422 Power-Off Measurement

The magnitude of the generator and protection device output leakage current (Ix) shall not exceed 100 microamperes. Refer to Figure 5, diagram F).

NOTE

The driver protection circuits guarantee a 16 volt clamp; drivers must not have parasitic latch up below 16 volts.

Figure 5: DEC422 - Generator Parameter Measurements

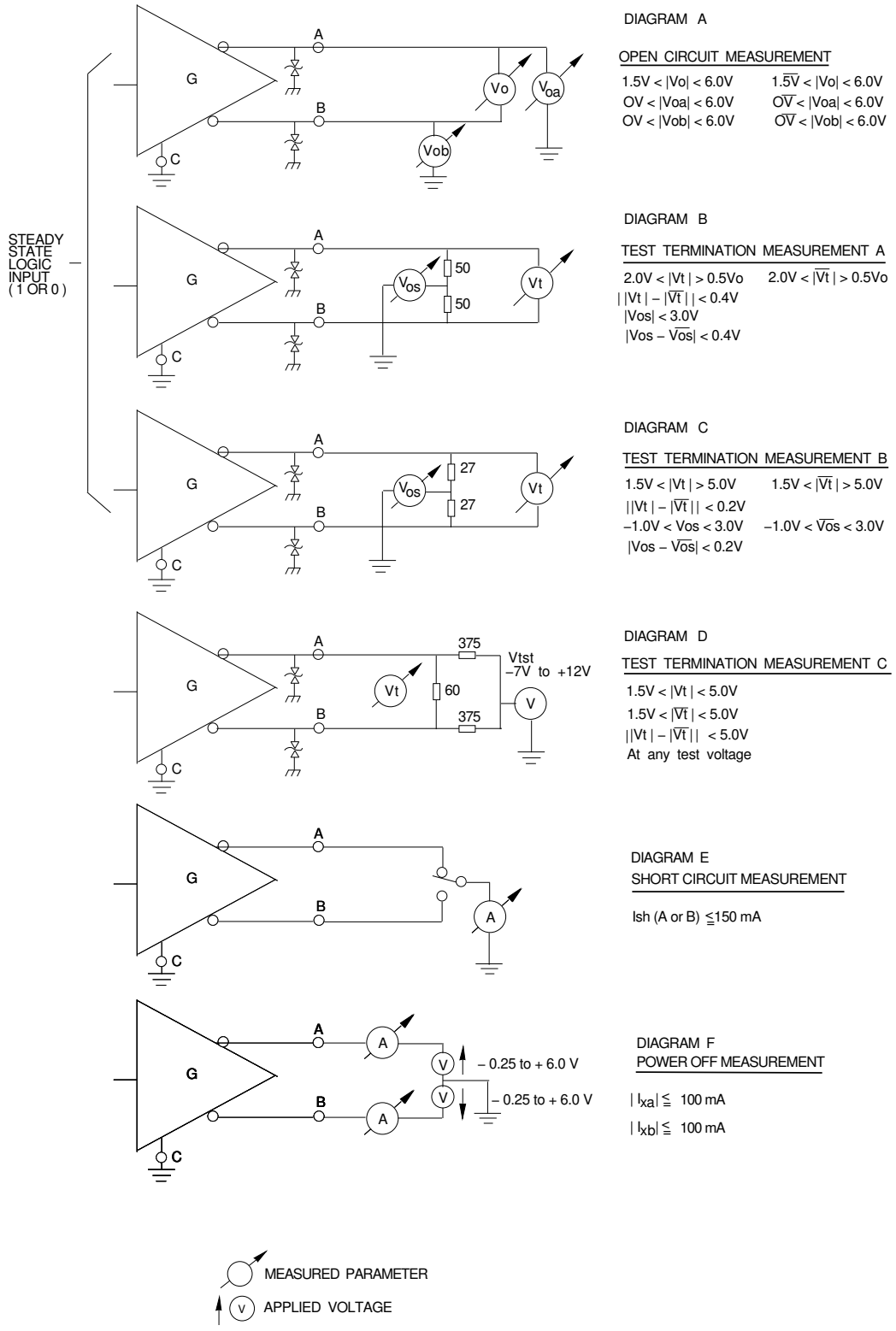


DIAGRAM A

OPEN CIRCUIT MEASUREMENT

1.5V < |Vo| < 6.0V 1.5$\overline{V}$ < |Vo| < 6.0V
OV < |Voa| < 6.0V O$\overline{V}$ < |Voa| < 6.0V
OV < |Vob| < 6.0V O$\overline{V}$ < |Vob| < 6.0V

DIAGRAM B

TEST TERMINATION MEASUREMENT A

2.0V < |Vt | > 0.5Vo 2.0V < |$\overline{Vt}$ | > 0.5Vo
| |Vt | – |$\overline{Vt}$ | | < 0.4V
|Vos| < 3.0V
|Vos – $\overline{Vos}$| < 0.4V

DIAGRAM C

TEST TERMINATION MEASUREMENT B

1.5V < |Vt | > 5.0V 1.5V < |$\overline{Vt}$ | > 5.0V
||Vt | – |$\overline{Vt}$ || < 0.2V
–1.0V < Vos < 3.0V –1.0V < $\overline{Vos}$ < 3.0V
|Vos – $\overline{Vos}$| < 0.2V

DIAGRAM D

TEST TERMINATION MEASUREMENT C

1.5V < |Vt | < 5.0V
1.5V < |$\overline{Vt}$ | < 5.0V
||Vt | – |$\overline{Vt}$ || < 5.0V
At any test voltage

DIAGRAM E

SHORT CIRCUIT MEASUREMENT

Ish (A or B) ≦150 mA

DIAGRAM F

POWER OFF MEASUREMENT

$|I_{xa}| \leqq$ 100 mA

$|I_{xb}| \leqq$ 100 mA

2.2.6 DEC422 Output Signal Waveform

The output signal waveform measurement will be made with a resistor of 54 ohms connected between points A and B (refer to Figure 5). A test signal composed of alternating ones and zeros shall be applied to the input. The change in amplitude of the output signal during transitions from one binary state to the other shall be monotonic between 0.1 and 0.9 of Vss. Thereafter, the signal voltage shall not vary more than 10% of Vss from the steady-state value, until the next binary transition occurs. The instantaneous magnitude of Vt shall neither exceed 5.0 volts, nor be less than 1.5 volts. Vss is defined as the voltage difference between the two steady-state values of the generator output.

2.2.7 DEC422 Waveshaping

Waveshaping of the generator output signal shall be used to control the level of interference (near-end crosstalk) that may be coupled to adjacent circuits in an interconnection. The rise time (tr) of the output signal shall be controlled to ensure the signal swings 0.1 to 0.9 Vss and reaches 0.9 Vss within 0.1 unit of tb or 20ns, whichever is greater, of the duration of the unit interval (tb) at the maximum data signaling rate to be used (per EIA 485).

2.3 LOAD CHARACTERISTICS

The load consists of one receiver (R) as shown in Figure 1. The electrical characteristics of a single receiver without a fail-safe provision are specified in terms of the measurements illustrated in Figures 6 through 8.

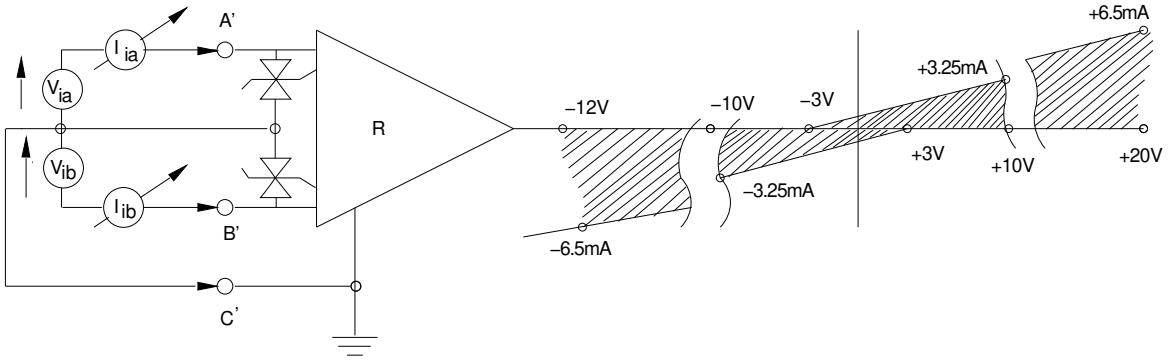
A circuit meeting these requirements results in a differential receiver having an impedance greater 4k ohms but less than 7k ohms, a small input threshold transition region between -0.2 and +0.2 volts, and allows for an internal bias voltage less than 2.0 volts in magnitude, or balanced biasing current with up to +/- 10 V bias.

The receiver used in the load for the unbalanced circuit is electrically identical to that specified for the balanced interface in EIA-423-A/DEC423.

2.3.1 Input Current-Voltage Measurements

The input current-voltage measurement shall be taken with the voltage Via (or Vib) ranging between -20 and +20 volts, while Vib (or Via) is held at 0 volts (grounded), the resultant input current Iia (or Iib) shall remain within the shaded region shown in the Figure 6. These measurements apply with the receiver's power supply(s) in both the power-off and power-on conditions.

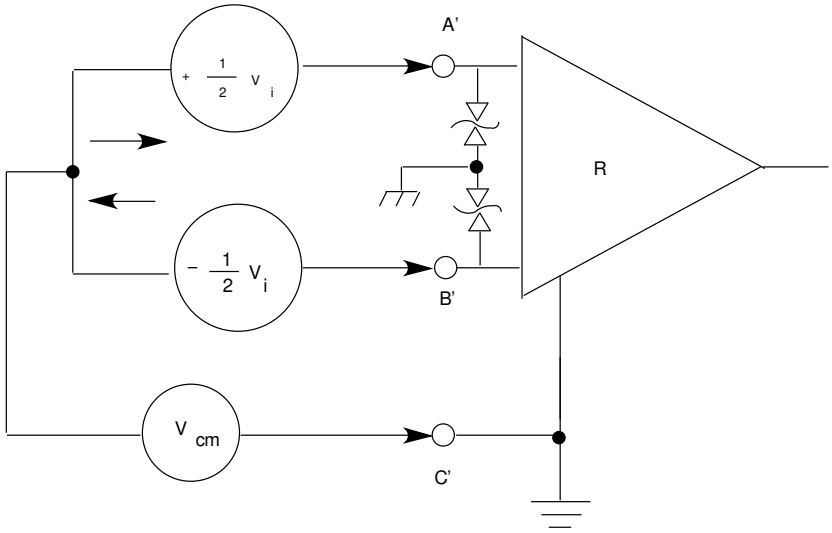
Figure 6: Receiver Input Current-Voltage Measurement



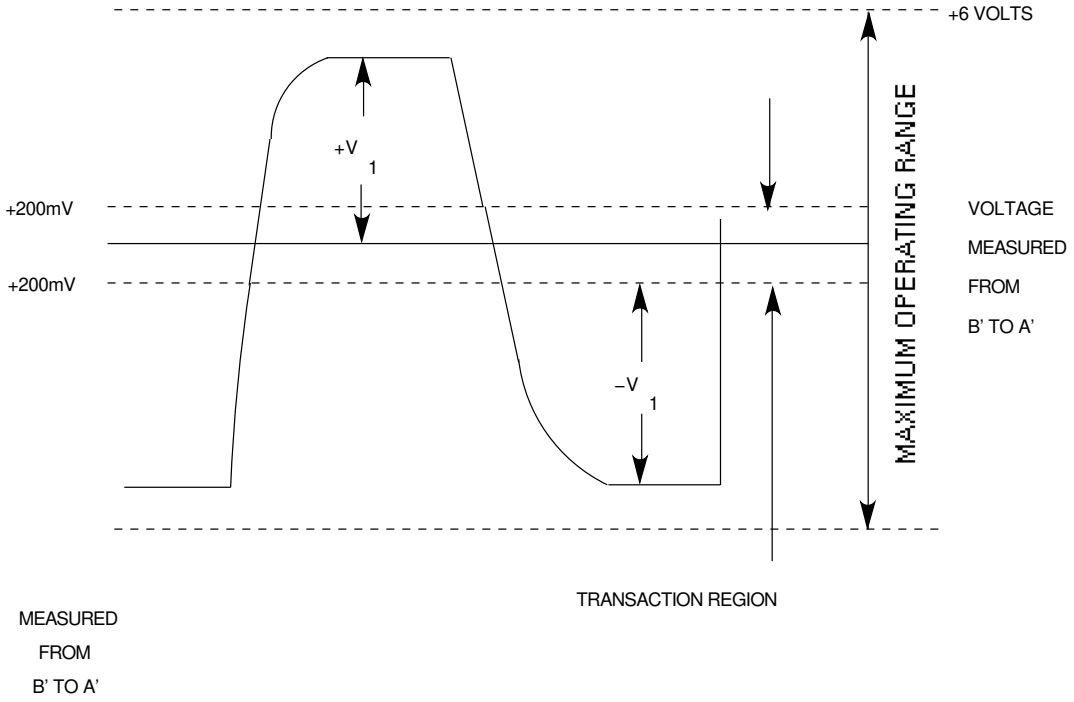
2.3.2 Input Sensitivity Measurement

The input sensitivity measurement shall be taken over an entire Common Mode voltage (Vcm) range of -7 to +7 volts (refer to Figure 7). The receiver shall not require a differential input voltage of more than 200 millivolts to recognize the intended binary state. The Common Mode voltage (Vcm) is defined as the algebraic mean of the two voltages appearing at the receiver input terminals (A' and B') with respect to the receiver zero reference point (C').

Figure 7: Receiver Input Sensitivity Measurement



V_{cm} = –7 to + 7 Volts



Reversing the polarity of Vi shall cause the receiver to assume the opposite binary state. The receiver is required to maintain correct operation for differential input signal voltages ranging between 200 millivolts and 6 volts in magnitude. The maximum voltage (signal plus Common Mode) between either receiver input terminal and receiver circuit ground shall not exceed 20 volts in magnitude or cause the receiver to operationally fail. Additionally, the receiver shall operate with a maximum differential signal of 15 volts applied across its input terminal when not in Common Mode.

The receiver must reject high frequency components in Normal Mode. A 1 volt peak-to-peak sine wave signal at a frequency of 5 MHz injected normal mode on a dc level of 0.3 volts must be rejected.

The receiver must reject high frequency components in Common Mode. A 5 volt peak-to-peak sine wave signal at a frequency of 5 MHz injected Common Mode on a dc level of 0.3 volts must be rejected. The output must not change.

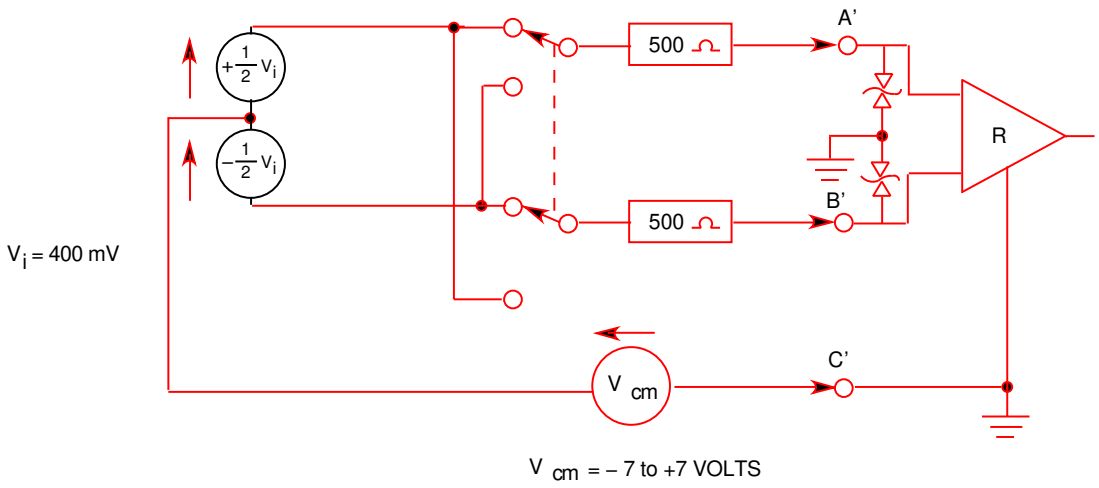
NOTE

Designers of terminating hardware should be aware that slow signal transitions with noise may produce instability or oscillatory conditions in the receiving device; therefore, appropriate techniques should be implemented to prevent such behavior. For example, hysteresis may be incorporated into the receiver to help prevent such conditions.

2.3.3 Input Balance Measurement

The balance of the receiver input voltage-current characteristics and bias voltages, shall ensure that the receiver will remain in the intended binary state when a differential voltage (Vi) of 400 millivolts is applied through 500 ohms to each input terminal, and Vcm is varied between -7 and +7 volts (refer to Figure 8). When the polarity of Vi is reversed, the opposite binary state shall be maintained under the same conditions.

Figure 8: Input Balance Measurement



2.3.4 Total Load Characteristics Limits

The total load, including multiple receivers and fail-safe provisions, shall have a resistance greater than 4k ohms between its input points (A' and B') and shall not require a differential input voltage of more than 200 millivolts for all receivers to recognize the intended binary state.

2.3.5 Fail-Safe Operation

Fail-safe operation standards and specifications using the electrical characteristics of the unbalanced voltage digital interface circuit may require that specific interchange leads be made fail-safe to certain fault conditions. Such fault conditions may include one or more of the following.

a. Generator in power-off condition (not met with current receivers). Receivers do not failsafe with DEC423 and EIA 232-D drivers, only DEC422 drivers. All DEC423 terminals and adapters from EIA 232-D must use either an active converter H3105, shorting device for system security and software loading.

NOTE

A new receiver has been defined, but has not been developed at this time. It will be put in this standard for all systems and terminal servers when it is available.

b. Receiver not interconnected with a generator

c. Open-circuited interconnecting cable

d. Short-circuited interconnecting cable

e. Input signal to the load remaining within the transition region (+/- 200 millivolts) for an abnormal period of time (application dependent). (not met with current receivers)

3 PROTECTION REQUIREMENTS

3.1 CIRCUIT PROTECTION

Unbalanced voltage digital interface generator and receiver devices, under either the power-on or power-off condition, complying with this standard shall not be damaged under the following conditions:

a. Generator open circuit.

b. Short-circuit between the signal conductor and signal return at either the generator or load interface.

c. Short-circuit to any other lead using electrical characteristics complying with this standard and EIA-422-A (Balanced Interface).

d. Short-circuit to ground.

4 TRANSIENT PROTECTION

Transient protection is necessary to protect Digital's products against damage from the effects of Electrical OverStress (EOS). This protection is mandated per the requirement stated in this document but also in DEC STD 122-0 *AC Power Line standard: Design Requirements and Guidelines*, and DEC STD 103-0 Electromagnetic Compatibility (EMC) Hardware Design Requirements).
DEC STD 122-0 defines the requirements for protection of AC power inputs from the effects of high voltage and current transients known as Electrical OverStress (EOS). Each product typically has two types of input; the power input and the data line input. When power inputs are fully protected as defined in DEC STD 122, data line inputs provide an alternate current path for transients. Therefore, data lines must meet similar protection requirements against EOS. DEC STD 122 addresses power inputs only; data line inputs are dealt with in this standard.

DEC STD 103 specifies ElectroStatic Discharge (ESD) testing to verify the immunity of completed Digital products to the effects of electrostatic discharge from human beings. This system is closed in that data and power cables are attached, and thus, transients are not inflicted directly into power and data lines. The testing is designed to guarantee functionality in most environments of usage: a typical carpeted office can generate ESD levels between 8 kV and 15 kV, with extreme situations generating ESD levels up to 39 kV. Drivers and receivers are very susceptible to ESD, and at best, are designed to withstand ESD levels of 2 Kv without additional protection. The ESD test procedures described in this standard are similar to those of DEC STD 103, but apply only to the active DEC423 or DEC422 signal pins on a connector.

DEC STD 052-4 testing is designed to fill the gaps left in DEC STD 122 and DEC STD 103 by guaranteeing immunity levels of data line inputs to the stresses of electrical overstress and electrostatic discharge.

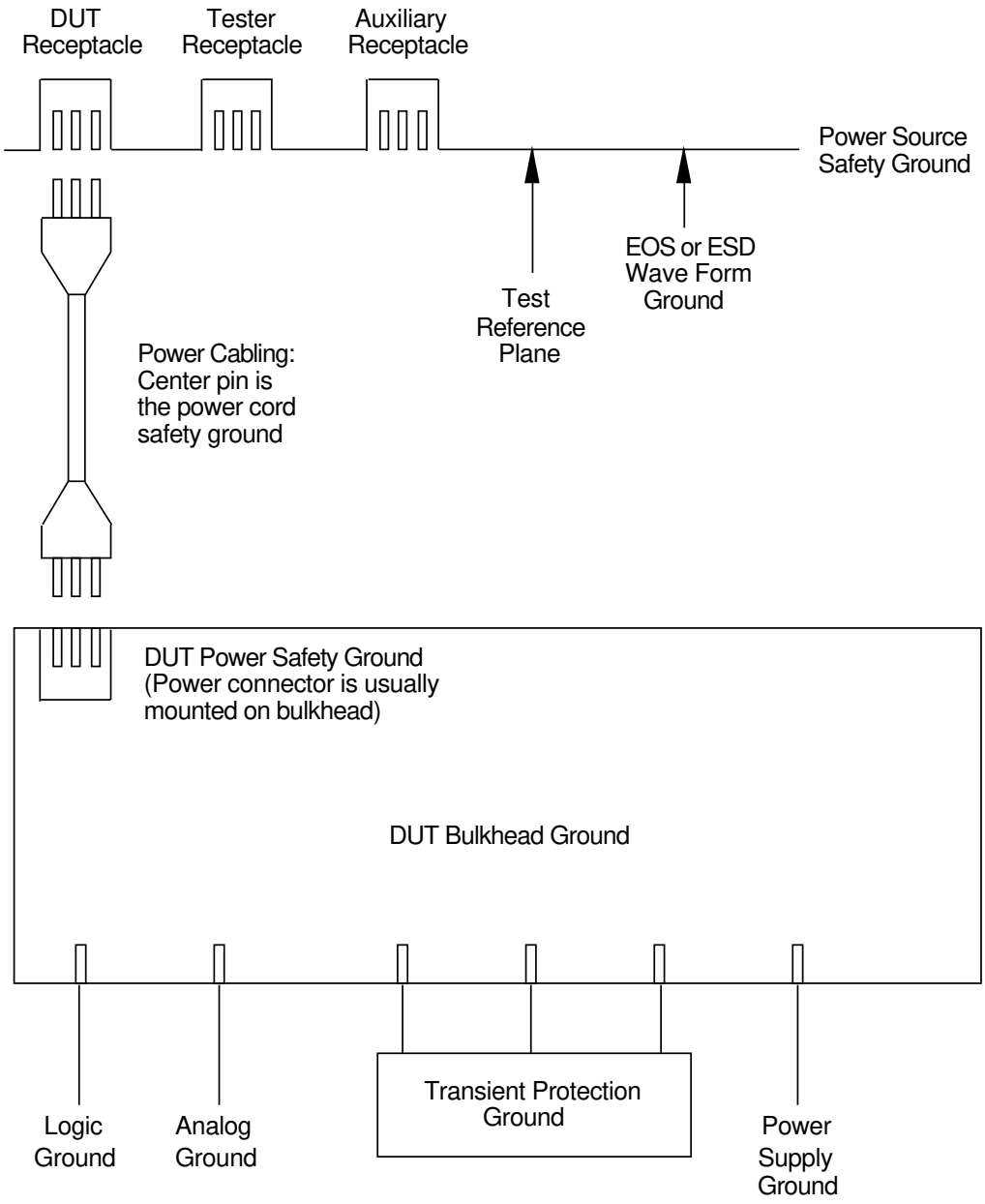
NOTE

DEC STD 122 and DEC STD 103 testing requirements apply to the entire product and must be complied with in addition to the requirements of this standard.

Grounding is a key element in transient protection. Some of the terms that are used to describe grounding are: reference plane, reference plate, safety reference, green or yellow wire reference pin, power plug safety reference pin, metal reference plate, bulkhead, power system safety ground, return, and chassis structure, to name a few. This standard deals with the following grounding terminology. Refer to Figure 9 for grounding configuration.

- Analog ground: The ground plane on an analog board.
- DUT bulkhead ground: Common area where logic ground, analog ground, power supply ground, transient protection ground and power system safety ground are tied; the system reference ground.
- DUT power safety ground: The green/yellow wire from the system which makes connection through the power cord safety ground to the power source safety ground.
- EOS or ESD test wave form ground: The reference for the test wave form; to be tied to the power source safety ground.
- Logic ground: The ground plane on a configured digital logic board. There may be more than one of these in the device under test (DUT).
- Power cord safety ground: Ground wire of a three wire power cord.
- Power source safety ground: The electrical power source and the building safety ground (usually this is eventually tied to a metal rod inserted directly into the earth).
- Power supply ground: The reference for internal power supplies.
- Test reference plane: the copper sheet that testing is done on; it is part of the test set-up and is tied directly to the power source safety ground.
- Transient protection ground: The separate ground on to which transient protection parts are grounded; in systems without a physical bulkhead, the transient protection ground to which all other grounds are attached acts as the bulkhead.

Figure 9: Grounding Configuration and Test Set-Up


DUT Receptacle
Tester Receptacle
Auxiliary Receptacle
Power Source Safety Ground
EOS or ESD Wave Form Ground
Test Reference Plane
Power Cabling: Center pin is the power cord safety ground
DUT Power Safety Ground (Power connector is usually mounted on bulkhead)
DUT Bulkhead Ground
Logic Ground
Analog Ground
Transient Protection Ground
Power Supply Ground

4.1 PROTECTION CRITERIA

No hardware damage is allowed during EOS and ESD tests.

Hard failures are events resulting in loss of DUT functionality and requiring operator intervention. Hard failures are acceptable during EOS testing. Hard failures are not acceptable during ESD testing.

Temporary loss of data line integrity (from which the system can recover without operator intervention) is acceptable during EOS and ESD testing.

4.2 EOS/ESD DAMAGE REDUCTION TECHNIQUES

NOTE

This standard is not written to provide design criteria for limiting EOS and ESD damage. For information on this, refer to Applications Note for Asynchronous EIA Interface Designs.

Damage to DEC423 and DEC422 drivers and receivers can be minimized by following the design rules:

a. All DUT grounds are referenced directly and individually to the DUT bulkhead ground. The DUT bulkhead ground is tied directly to the power source safety ground via the power cord safety ground.

b. Use transient protection parts to limit voltage transients on driver outputs and receiver inputs from common mode and normal mode sources. Recommended parts are described in Appendix B.

c. Mount the transient protection parts as close as possible to the data line connector(s), and locate them between the data line connector(s), and the drivers/receivers which they protect.

d. A separate ground for the transient protection parts may be necessary. This transient protection ground shall be tied directly to the DUT bulkhead ground, or, in the absence of a bulkhead, should act as the common grounding point for all other DUT grounds.

e. Connect conductive data line connector shells directly to the bulkhead.

f. Driver and receiver ground pins should be directly connected to the logic ground.

g. Create as much ground etch area as possible around the data line connector, beneath the transient protection parts, and close to the drivers and receivers.

h. When using transient suppressers in integrated circuit (IC) packages, run the ground etch under the package. This will prevent EOS and ESD spikes from crossing from input to output pins.

NOTE

Transient suppresser IC packages are made with input pins on one side and output pins on the other side. The four corner pins of the package are ground pins, and all four pins must be tied directly to ground (either transient protection ground or logic ground). Individual transient protection parts must be carefully placed to accomplish the above.

i. Use of filter-connectors is optional. Filter connectors may provide added EOS/ESD protection by slowing the leading edge of pulses.

4.3 EOS TEST PROCEDURES

4.3.1 DUT SET-UP

The device under test (DUT) is any system set up with the DEC423 or DEC422 data line communication system. The grounding configuration and test set-up is shown in Figure 9.

NOTE

Active pins are any pin that is attached to any board inside the system. Whether these pins actually carry a signal or are simply attached to ground through a resistor, they are to be treated as active and tested as such. Inactive pins are defined as those that are not attached to anything.

To facilitate access to the active pins, a cable stub with mating connector may be used. The cable stub should be less than 9 cm (4 inches) in length. The individual wires of the stub corresponding to each active pin are probed to perform the required tests. All lines not under test are left open.

The chassis of the DUT is never grounded to the test reference plane. If the DUT has an exposed metal construction, it should be isolated above the test reference plane by at least 10 mm (0.5 inch).

NOTE

Keep all grounding connections and the cable stub as short in length as possible during testing.

4.3.2 TEST EQUIPMENT SETUP

To establish the ground of the test set-up, the test reference plane is tied directly to the power source safety ground. This configuration is unchanged for all testing.

The reference plane should extend a minimum of 250 mm (10 inches) beyond the vertical edge of the product.

The EOS tester shall be capable of supplying the following wave forms and amplitudes:

a. An 8 x 20 microsecond IEEE 587B wave form, current set to 40 amperes and voltage limited to 1500V.

b. An EOS Oscillatory wave form of 100 kHz and 0.5 microsecond rise time (IEEE 587B wave form), current set to 40 amperes and voltage limited to 3 kV.

c. An 8 x 20 microsecond wave form (IEEE 587B wave form), current set to 200 amperes and voltage limited to 1500V.

d. The tester shall be set up with the probe attached to the active pin(s) to be tested and the tester wave form ground attached to the power source safety ground.

4.3.3 TEST METHOD

All tests shall be done to all active pins on the DEC423 and DEC422 interfaces.

Test wave forms a. and b. (as listed in subhead 4.3.2) shall be done with all (active and non-active) pins not under test left open.

Test wave form c. shall be applied simultaneously through ten-ohm resistors to all active pins (minimum of eight required). If fewer than eight active pins are available on the product, adjust the current setting of the tester so that the maximum current per line shall not exceed 40 amperes.

All tests shall be done in both positive and negative polarities.

All tests shall be done with the equipment in both powered on and powered off states.

NOTE

Powered on testing is done with the DUT power cabling attached and the power switch on. Powered off testing is done with the power cabling attached and the power switch off. If the DUT can not be powered off without detaching the power cable, attach the ground pin of the power cable to the power source safety ground.

All tests shall be applied 5 times to each pin.

5 ESD TEST PROCEDURES

5.1 DUT SET-UP

DUT set-up is the same as for EOS testing.

NOTE

Active pins are any pin that is attached to the boards inside the system. Whether these pins actually carry a signal or are just attached to ground through a resistor, they are to be treated as active and tested as such. Inactive pins are defined as those that are not attached to anything.

5.2 TEST EQUIPMENT SET-UP

Relative humidity and temperature shall be recorded. Recommended environmental conditions for testing are at 50% +/- 2% RH, and 23°C +/- 2°C.

The ESD tester shall be capable of the following wave form: the IEC 801.2 Part 2: ESD Requirements wave form. It shall have a discharge network of 330 Ohms and 150pF and a metallic ball discharge tip.

The tester shall be set up with the tester wave form ground attached to the power source safety ground.

5.2.1 TEST METHOD

Tests shall be done to all active pins on the DEC423 and DEC422 interfaces.

ESD surge levels are 2kV, 4kV, 6kV, 8kV, 10kV, 12kV and 15kV.

ESD testing shall be done with all (active and non-active) pins not under test left open.

ESD discharges shall be applied five times to each active pin.

All tests shall be done to all active pins in both polarities.

All tests shall be done with the equipment in both powered up and powered down states.

NOTE

Powered on testing is done with the DUT power cabling attached and the power switch on. Powered off testing is done with the power cabling attached and the power switch off. If the DUT can not be powered off without detaching the power cable, attach the ground pin of the power cable to the power source safety ground.

The approach speed should simulate a person reaching to touch a pin. The purpose of this test is to duplicate reality in a human discharging to a pin. This is equal to approximately 30 cm/s (12 inches/s). The sequence of tests is to test each surge level in both polarities. In effect, the test would run, +2kV, -2kV, +4kV, -4kV, and so on.

6 FILTERING REQUIREMENTS

Digital products using direct connect interface devices must pass FCC Part 15J emissions testing with unshielded cable as specified in DEC STD 103-0. To comply with DEC STD 103-0, a product must first pass tests for conducted and radiated Electromagnetic Interference (EMI). This standard requires data conductors to be measured on all unshielded data conductors, and radiated measurements for EMI generated from the following sources.

a. Signal sources

b. The cable antenna effect

c. Module Common Mode voltage

6.1 APPLICATION INFORMATION

Traditionally, Digital system designers have mounted communications interfaces within a cabinet and run a piece of flat gray cable from the interface to a bulkhead or distribution panel affixed to the rear of the cabinet. However, the flat gray cable picks up emissions within the cabinet and radiates them outside and vice versa. The following process should be performed to ensure that products using this standard meet the requirements of DEC STD 103-0.

For systems with a distribution panel, mount the direct connect drivers and receivers directly behind the distribution panel/bulkhead. For systems where the module handle is designed to be part of the bulkhead, with the connectors mounted on the handle, the drivers and receivers should be mounted on the module. Connect protection devices and filter connectors directly to the bulkhead reference. The filter connectors may not be required, depending on system noise, layout, and the speed of the protection devices.

Layout and design rules to minimize the effects of radiated EMI are as follows. The numbers in parentheses indicate the EMI radiation source that each rule addresses.

- Use rise-time-controlled drivers. (1)
- The reference plane described for EOS/ESD protection is also a good Radio Frequency (RF) reference plane. Locate drivers and receivers as close as possible to this plane. (3)
- Minimize the distance between the output connector and the driver outputs or receiver inputs. (2)
- Bypass the power to the drivers and receivers with short capacitor leads to the reference plane. (3)
- Establish a single reference at the bulkhead for the power supply common, green/yellow wire ground, and driver and receiver signal reference. (3)

7 CONNECTORS

This standard defines two connectors for use with Digital products providing DEC423 and DEC422 direct connections. Recommended connectors are described in Appendix B.

a. The Modified Modular Connector (MMC), either a male Modified Modular Plug (MMP) or a female Modified Modular Jack (MMJ).

b. The 36-pin Champ™ connector.

7.1 CONNECTOR PINNING

7.1.1 The Modified Modular Jack (MMJ)

The pinning used for the MMJ, Digital part number 12-23433-00, shall be as shown in Table 1.

Table 1: Pinning for The Modified Modular Jack

Pin	Signal	Direction
1	Ready Out (optional)	Out
2	Transmit Data +	Out
3	Transmit Data - (Send Common)	Out
4	Receive Data -	In
5	Receive Data +	In
6	Ready In (Optional)	In

Pin 1 and pin 6 are only active with printer ports; they are not compatible with DEC422. DEC423 system and terminal server applications should only use the high impedance receiver for pin 6, with a program disabled feature for use on DEC422 applications.

When the MMJ is used in applications using Ready Out (pin 1) and Ready In (pin 6), Figure 10 shows how the MMJ interface would be configured using DEC423 drivers and receivers (protection devices not shown). The signal attached to pin 1 must be an outbound signal and will use pin 3, Transmit Data - (Send Common), as a reference. The signal attached to pin 6 must be an inbound signal and will use pin 4, Receive Data - (Receive Common), as a reference. The two IN/OUT restrictions are required for the male-male connecting cables perform a "null-modem" function. This configuration is recommended for local terminal-to-printer connections using MMCs.

™ The 36-pin Champ™ connector is a registered trademark of Amp Inc.

Figure 10: DEC 423 Configuration for Ready Out/In Active (Printer Control Connection)

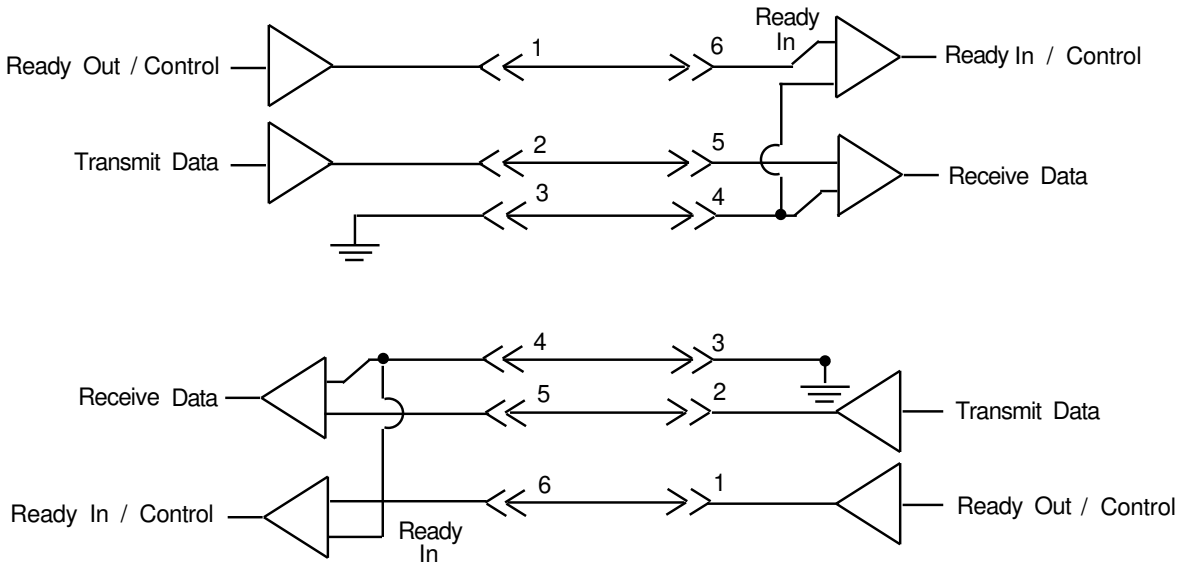
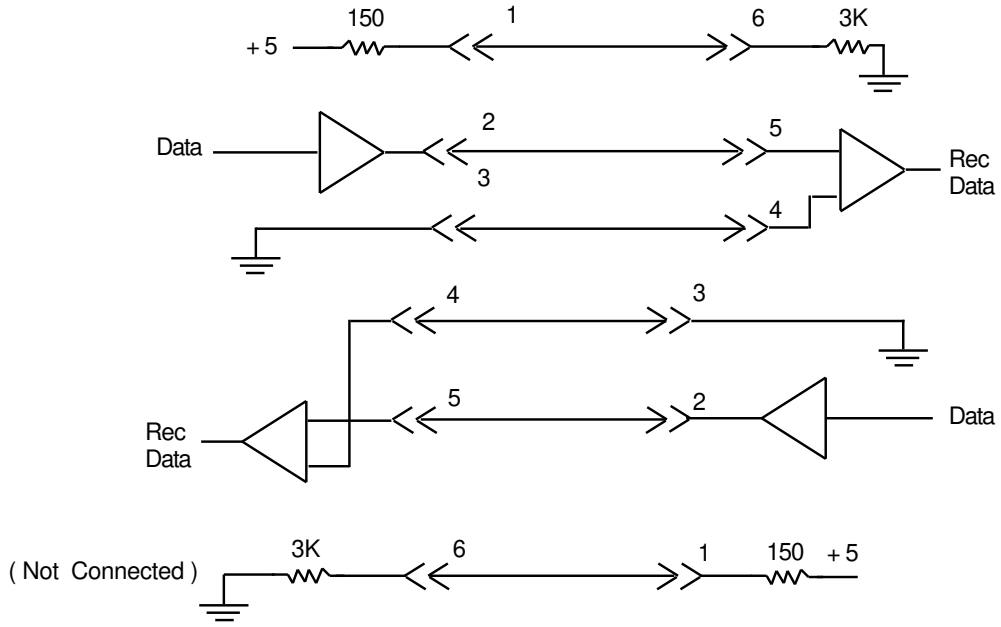


Figure 11 shows how unused lines should be terminated to reduce noise pickup and prevent ESD problems, and shows where to place the lines in an expected logic state for the control lines. Pin 1 must be driven by an active device or terminated by a 150-ohm resistor to +5 volts. A protection device must be included to protect the +5 volt supply. Pin 6 must be connected to a receiver or terminated with a 3 K ohm resistor to frame ground. Since a metal film resistor would be destroyed by EOS/ESD transients, a 1/2-watt carbon composition resistor is required.

Figure 11: DEC 423 - Data Only Connection



Failsafing of pin 6 is required if implemented on a printer port to detect a powered down printer. Refer to Appendix B for recommended components.

Referring to Figures 10 and 11, note that using pins 1 and 6 with shared commons may reduce speed-versus-distance performance and preclude direct interconnection to EIA-422-A circuits. This means any printer, printer port, or any other device implementing an active receiver on Pin 6 must not be connected to EIA 422-A/V.11 interfaces. Wiring of pins 1 and 6 is looped back in the modified modular connector at a wall mount box or cable concentrator. Refer to Appendix D for descriptions of the latter devices.

NOTE

As of November 1989 all wiring installations have Pin 1 looped back to pin 6. Worldwide building wiring standards are evolving to have four pairs for each terminal, wired pin 1 to pin 1, and the like. Future provisions may carry pin 1 (Ready Out) to the remote end. One Digital product, a DECServer 300, uses all six wires, where 1 and 6 are for flow control and status.

7.1.2 The 36-Pin Champ™ Connector

The pinning used for the 36-Pin connector shall be as shown in Table 2.

All 36-pin cabling provides a straight-through connection. The signal names reflect the host names.

Reserved pins must be terminated at the system end with a 150-ohm resistor to frame ground.

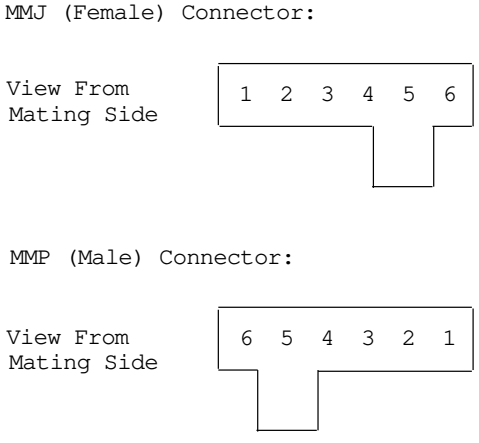
Table 2: Pinning for the 36-Pin Champ™ Connector

1 Blu/Wht	Line 0 Transmit +	19 Wht/Blu	Line 0 Transmit -
2 Org/Wht	Line 0 Receive +	20 Wht/Org	Line 0 Receive -
3 Grn/Wht	Line 1 Transmit +	21 Wht/Grn	Line 1 Transmit -
4 Slt/Wht	Line 1 Receive +	22 Wht/Org	Line 1 Receive -
5 Blu/Red	Line 2 Transmit +	23 Wht/Slt	Line 2 Transmit -
6 Blu/Red	Line 2 Receive +	24 Red/Blu	Line 2 Receive -
7 Org/Red	Line 3 Transmit +	25 Red/Org	Line 3 Transmit -
8 Grn/Red	Line 3 Receive +	26 Red/Grn	Line 3 Receive -
9 Brn/Red	Line 4 Transmit +	27 Red/Brn	Line 4 Transmit -
10 Slt/Red	Line 4 Receive +	28 Red/Slt	Line 4 Receive -
11 Blu/Blk	Line 5 Transmit +	29 Blk/Blu	Line 5 Transmit -
12 Org/Blk	Line 5 Receive +	30 Blk/Org	Line 5 Receive -
13 Grn/Blk	Line 6 Transmit +	31 Blk/Grn	Line 6 Transmit -
14 Org/Blk	Line 6 Receive +	32 Blk/Brn	Line 6 Receive -
15 Slt/Blk	Line 7 Transmit +	33 Blk/Slt	Line 7 Transmit -
16 Org/Yel	Line 7 Receive +	34 Yel/Blu	Line 7 Receive -
17 Org/Yel	Reserved	35 Yel/Org	Reserved
18 Org/Yel	Reserved	36 Yel/Grn	Reserved

7.2 CONNECTOR PHYSICAL PIN POSITIONS

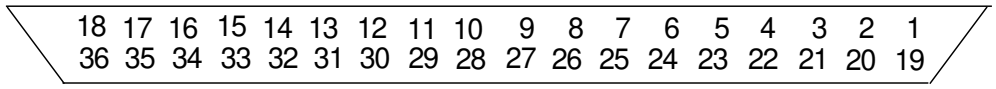
The following figures indicate the pinning convention for the Modified Modular Connector as viewed from the mating side.

Figure 12: Modified Modular Connector Pinning Conventions (Male and Female)



The following figures indicate the pinning convention for the 36-pin Champ™ female connector viewed from the mating side.

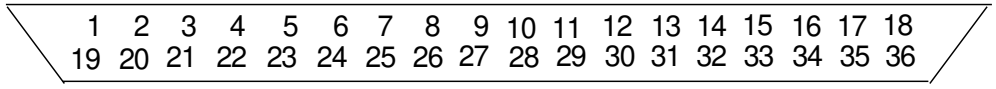
Figure 13: 36-Pin Champ™ Connector Pinning Conventions (Female)



VIEW FROM MATING SIDE

The 36-pin Champ™ male connector on a product with active devices must have a metal-shield connector connected to the system reference (logic, chassis, and earth reference point) to provide for the use of shielded cable.

Figure 14: 36-Pin Champ™ Connector Pinning Conventions (Male)



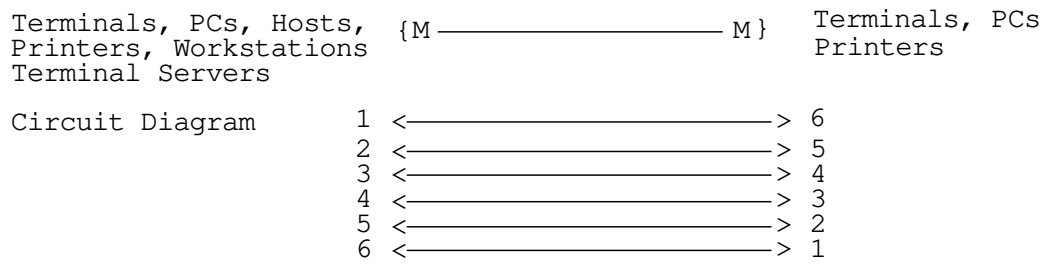
VIEW FROM MATING SIDE

8 CABLING FOR LOCAL DIRECT CONNECTIONS

8.1 6-CONDUCTOR TERMINAL INTERCONNECTION FLAT CABLE

The DEC423 speed/distance performance is limited when using a flat terminal interconnection cable because it is a flat cable instead of a twisted pair cable, and is therefore more susceptible to noise pickup. The environment limits the cable length. This cable is designed to be user-installable and user-removable, and resembles the mounting cord of a conventional telephone set. A drawing and circuit diagram of the cable are shown in Figure 15.

Figure 15: Flat, 6-Conductor Terminal Interconnection Cable



Note that the cable is terminated on both ends by an MMP (male) connector. In the modified modular connector scheme, all MMJ (female) connectors receive signals on pins 4, 5, and 6 and transmit signals on pins 1, 2, and 3. The cable in Figure 15 performs a "null modem" function, transposing signals received on pin 6 to pin 1, preserving this convention.

8.2 BUILDING WIRING

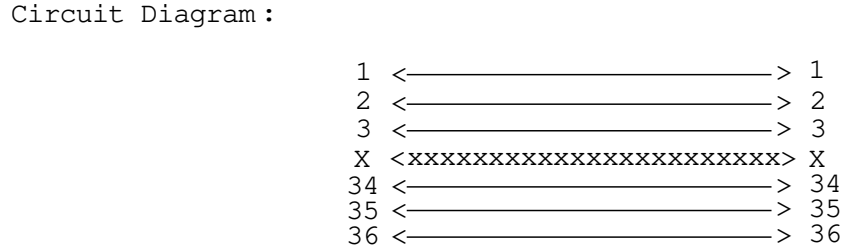
When building wiring is required, terminal interconnection cable is used to reach an MMJ located in a wall mount box (see Appendix B). From the wall mount box MMJ, this standard recommends using two-pair, twisted-pair, 24-gauge copper wire with 20 to 26 ohms per 1000 feet and less than 20 pF per foot capacitance for single-line wiring. Shielding should be avoided if possible; shielding increases the capacitance of the cable, reducing the distance that can be driven.

The building wiring must not contain any crossovers. Refer to subhead 4.6.1.1 for more information.

8.3 36-CONDUCTOR CABLE FOR MULTIPLE LINES

A cable with a male 36-pin Champ™ connector at each end may be used to connect devices located up to 250 feet apart. In a typical application, multiple terminals are connected to a computer using this cable assembly and other DECconnect products described in Appendix B. This cable is a straight-through connector with pin 1 corresponding to pin 1, pin 2 corresponding to pin 2, and so on, as shown in Figure 16.

Figure 16: Multiple Line Connections



8.4 INTERCONNECTING CABLE CHARACTERISTICS

The speed and distance attainable using the drivers and receivers specified in this standard are dependent on the characteristics of the interconnecting cable. Appendix B provides guidance on performance and cable length versus data signaling rate for cables recommended for use with this standard and for cross-connection to EIA 232-D and EIA 422-A. Adapters developed to provide cross-connection to EIA 232-D interfaces are described in Appendix D.

GLOSSARY

common mode (Vcm): The voltage difference between the average voltage and the reference voltage of the receiver.

creepage distance: This is the IEC term for what UL refers to as "over-surface" spacing.

failsafe: This is a term used for the biasing or control of the input to the receiver. The receiver output is a known state, for data. When the input is left open, the output will go to a mark state, holding the UART in a hold state. Each line is failsafed according to its function. The 75146 failsafe resistors perform a dual function. Not only is the receiver at the known state, but the input impedance is brought into range to meet EIA 232 and V.28 specifications.

failsafe negative: Holding the line in the "off" state, differentially holding or changing the thresholds, which guarantees the state of the line. The failsafe state occurs when nothing is connected to the receiver or the driver is powered down.

failsafe positive: Holding the line in the "on" state, differentially holding or changing the thresholds, which guarantees the state of the line. The failsafe state occurs when nothing is connected to the receiver or the driver is powered down.

IEC: International Electrotechnical Commission

Insertion Loss: The amount the signal is decreased after passing through the device.

Normal Mode: The voltage placed directly across the input terminals of the differential receiver.

slew rate: Because the line drivers used have trapezoidal outputs, the rise and fall time of these drivers is controlled by a slew-rate resistor. The slew rate is the time it takes for the signal to transition between 10% and 90% of the full swing of the signal. Also referred to as Risetime control.

UL: Underwriters Laboratories (USA)

VDE: Verband Deutscher Electrotechniker - regulatory agency

APPENDIX A REFERENCED DOCUMENTS

A.1 EL-Class Digital Documents

EL-Class Number	Document Title
EL-00052-01	*DEC STD 052-1 Operational Requirements for Serial Data Terminal Equipment and Serial System Interfaces Operating as DTEs Connected to EIA RS-232-C or CCITT V.28 Point-To-Point Modems or Data Service Units*
EL-00052-02	*DEC STD 052-2 Electrical Requirements for Binary Interfaces That Conform to EIA RS-232-C or CCITT V.28 Modems*
EL-00066-02	*DEC STD 066-2 Waivers to Digital Design Standards*
EL-00103-00	*DEC STD 103-0 Electromagnetic Compatibility (EMC) - Overview and Process Requirements*
EL-00122-00	*DEC STD 122-0 AC Power Line Standard: Design Requirements and Guidelines*

Use VTX SMC to order copies of EL-class documents from Standards and Methods Control. Send distribution questions to JOKUR::SMC or call DTN: 234-4423.

A.2 Other Digital Documents

Document Number	Document Title
EK-EIADS-HM-001	*Design Guidelines for Serial Asynchronous Interface*

A.3 Other Documents

Document Number	Document Title
CCITT (V.10)	*External Characteristics for V.10 Unbalanced Double-Current Interchange Circuits for General Use With Integrated Circuit Equipment in the Field of Data Communications*
CCITT (V.24)	*List of Definitions for V.24 Interchange Circuits Between Data Terminal Equipment and Data Circuit Terminating Equipment*
CCITT (V.28)	*Electrical Characteristics for V.28 Unbalanced Double-Current Interchange Circuits*
EIA 232-D	*Interface Between Data Terminal Equipment and Data Communication Equipment Employing Serial Binary Data Interchange*
EIA 422-A	*Electrical Characteristics of Balanced Voltage Digital Interface Circuits*
EIA 423-A	*Electrical Characteristics of Unbalanced Voltage Digital Interface Circuits*
EIA 485	*Electrical Characteristics of Generators and Receivers for use in Balanced Digital Multi Point Systems*
IEC 801.2	*Electrostatic Compatability for Industrial-Process Measurement and Control Equipment, Part 2: Electrostatic Discharge Requirements*

A.4 Ordering Information

Copies of CCITT documents are available from the International Telecommunications Union, Secretariat CCITT, Place Des Nations CH - 1211 Geneve 20, Switzerland, Tel. +41 22 99 51 11, Telex 421000 (UIT CH).

Copies of EIA documents are available from the Electronic Industries Association, 2001 Eye Street, NW, Washington, DC 20006, USA, 202-457-4900.

Copies of IEC documents may be obtained from the American National Standards Institute, 1430 Broadway, New York, NY 10018, telephone (212) 354-3300 x479.

Copies of EK-EIADS-HM-001 are available from Ralph Dieter, ENET: WORDS::DIETER.

APPENDIX B COMPONENTS THAT MEET THE REQUIREMENTS OF DEC STD 052-4

B.1 DRIVERS AND RECEIVERS

The drivers and receivers listed in Tables 3 and 4 meet the requirements of this standard and are recommended for asynchronous interface applications. Note that the 5170 driver is to be replaced by the 5170A driver and that the 9639 has been replaced by the 75146. These chips are being redesigned to Digital specifications to provide superior performance and less susceptibility to EOS/ESD. In the case of the 5170A driver, it is being designed to use the same protection devices as the receivers (see Table 5). This will facilitate component layout and potentially reduce the required number of protection packages.

When using discrete protection devices (see Table 6), the use of a 33 microHenry inductor, Digital part number 16-01759-00, is optionally recommended for filtering and to act as a fuse element. Further details on these components and how to properly incorporate them into new designs is contained in EK-EIADS-HM-001 *Design Guidelines for Serial Asynchronous Interfaces*.

Table 3: Recommended DEC423 Drivers and Slew Rate Resistors

Industry Part Number	Digital Part Number	Units Per Device	Slew Rate Resistance (k ohms)	
			DEC423	EIA 232-D/V.10
9636	19-15415-00/B0	Dual	47	27.0
5170*	19-23889-01/02	Octal	10	5.3
5170A*	19-32475-01/02	Octal	10	5.3

* To be phased out by the 5170A by 01-June-1990.

Table 4: Recommended DEC422 Drivers

Industry Part Number	Digital Part Number	Units Per Device
96172	19-27442-01	Quad

Table 5: Recommended DEC423/EIA232-A/DEC422 Receivers (with Built-in Filters)

Industry Part Number	Digital Part Number	Units Per Device
75146	19-27782-01	Dual
5180	19-23890-03/04	Octa

Table 6: Recommended Protection Devices

Industry Part Number	Vendor Part Number	Digital Part Number	Units Per Device
9636	SA7.0CA	11-26859-01	Discrete
		19-25894-02	Octal
5170	SA7.0CA	11-26859-01	Discrete
		19-25894-02	Octal
5170A	P6KE22CA	11-27643-02	Discrete
		19-25894-01	Octal
75146	P6KE22CA	11-27643-02	Discrete
		19-25894-01	Octal
5180	P6KE22CA	11-27643-02	Discrete
		19-25894-01	Octal
96172	SA7.0CA	11-26859-01	Discrete
		19-25894-02	Octal

B.2 CONNECTORS AND CABLES

The Modified Modular Connectors used with this standard are as follows:

- Female Modified Modular Jack (MMJ) - Digital Part Number 12-23433-00
- Male Modified Modular Plug (MMP) - Digital Part Number 12-23432-00

A flat, 6-Conductor Terminal Interconnection Cable using MMPs is designated BC16E.

The following list are several versions of the 36-pin Champ™ connector.

- Filtered, straight, female connector - Digital Part Number 12-25069-01
- Filtered, right-angle, female connector - Digital Part Number 12-25331-01
- Filtered, right-angle, SBOX female connector - Digital Part Number 12-30090-01
- Unfiltered, right-angle, female connector - Digital Part Number 12-25147-01

The male Champ™ connector can only be obtained as part of a cable assembly; BC16C/D is the shielded version and BC16H/J is the unshielded version. The cable pinning is connected straight through, for example, pin 1 to pin 1, pin 2 to pin 2, and so on.

A complete listing and description of these and other components associated with this standard are described in the *DECconnect System Planning and Configuration Guide*.

APPENDIX C SYSTEM INTERFACE AND CABLE LIMITATIONS

When using equipment with DEC423 and DEC422 interfaces, consideration should be given to some of the problems that may be encountered due to the interconnecting cable characteristics, cable length, generation of near-end crosstalk, and interconnection with interfaces using other electrical characteristics.

C.1 OPERATIONAL CONSTRAINTS

The maximum operating distance for the unbalanced voltage digital interface is primarily a function of the amount of interference (near-end crosstalk) coupled to adjacent circuits in the equipment interconnection. Additionally, the unbalanced circuit is susceptible to exposure to differential noise resulting from any imbalance between the signal conductor and signal return at the load interface point.

Increasing the interconnection cable length between the generator and load interface points increases the exposure to common mode noise and the amount of near-end crosstalk. Accordingly, users are advised to restrict the cable length to a minimum, consistent with the generator-load physical separation requirements.

Several curves for data rate versus cable length for DEC423 are given in Figure 17. Each curve depends on the type of cable or cables used and signaling used, For example, EIA 423-A or EIA 232-D.

Curve A is based on the curves shown in Figure 17 of the Appendix to EIA 423-A, Guidelines for Application, for the special case where linear waveshaping is recommended as per DEC423. The curve is arbitrarily cut at 40 kbps, the maximum distance recommended by DEC423. EIA 423-A based its curves upon calculations and empirical data using twisted pair, copper, telephone cable with a shunt capacitance of 52.5 pF/meter (16 pF/ft), a 50-ohm source impedance, a 12 volt peak-to-peak source signal, and allowing a maximum near-end crosstalk of 1 volt peak.

Curve A in Figure 17 does not account for common mode noise coupled to the circuit from other sources. The effects of near-end crosstalk influence the cable length limits long before any signal quality degradation will impact the performance. Under these conditions, a zero crossing ambiguity of less than .05 of a bit time will be realized.

Cables having characteristics different from the twisted-pair, 24 AWG, 52.5 pF/meter (16 pF/ft) cable, can also be used; however, the user should determine that the crosstalk will be held to the suggested value of less than one volt. The type and length of cable used must be capable of maintaining the necessary signal quality needed for the particular application.

Curves B and C indicate the recommended speed/distance limits when using cables or combinations of cables specified for use by the DECconnect System. Curves B and C are based on empirical crosstalk data compiled for the cables shown with each curve in Figure 17, assuming that the drivers, receivers, and protection devices are those specified in Appendix B, and that the cabling conforms to the requirements of this standard. For Curve

B, flat cable and 18-pair, shielded cable can be combined up to a distance of 300 meters, however, the shielded cable segment shall not exceed the 90 meter limit of Curve C.

Curve D is the speed/distance curve for DEC423 drivers/receivers configured for EIA 232-D or for DEC423 interconnected with EIA 232-D. This distance is based on the EIA 232-D recommendation that the maximum capacitance of the generator to receiver circuit be 2500 pF. Assuming a 24 AWG twisted-pair, 65.6 pF/meter (20 pF/ft) cable is used with a combination receiver/protection device capacitance equal to or less than 500 pF, the maximum distance attainable without violating EIA 232-D is 30 meters. Most telephone cable manufacturers make unshielded, twisted-pair wire that meets or exceeds 65.6 pF/meter so that this limit is easily meet. The 30 meter distance may be exceeded as long as the 2500 pF restriction is satisfied. The maximum speed recommended by EIA 232-D is 20 kbps, therefore, the curve is ended at this point.

C.2 COMPATIBILITY WITH OTHER INTERFACES

C.2.1 COMPATIBILITY OF DEC423 AND EIA 422-A/V.11/DEC422 IN THE SAME INTERFACE

Drivers and receivers meeting the requirements of DEC423 are compatible with those meeting EIA 422-A/V.11/DEC422. The electrical characteristics of the unbalanced voltage digital interface are designed to allow use of both balanced and unbalanced circuits within the same interconnection cable sheath. For example, the balanced circuits may be used for data and timing while the unbalanced circuits may be used for low speed control functions.

C.2.2 DEC423 INTERCONNECTION WITH EIA 422-A/V.11/DEC422

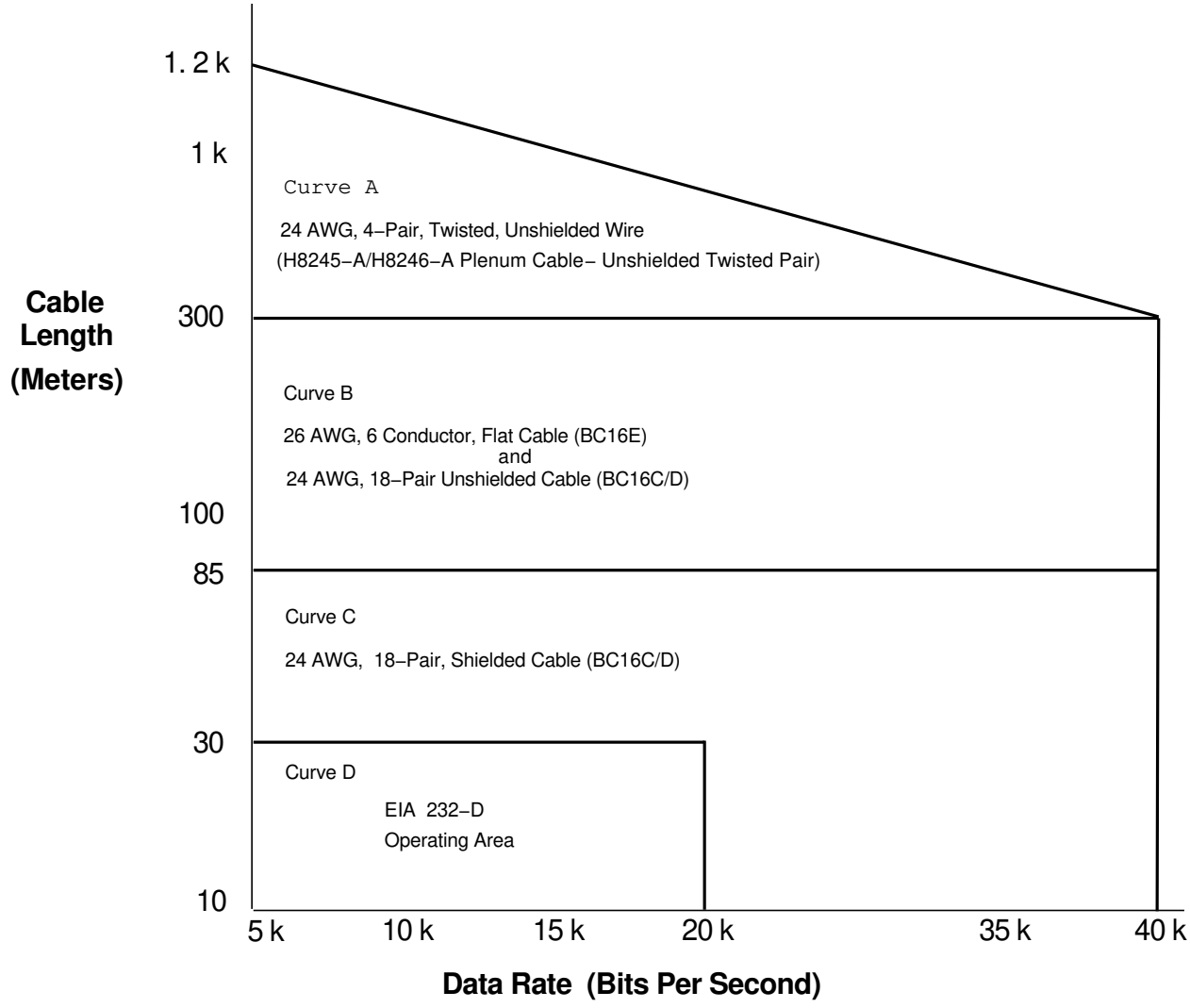
Since the basic differential receivers of DEC423 and EIA 422-A/V.11/DEC422 are electrically identical, it is possible to interconnect an equipment using DEC423 receivers and drivers on one side of the interface with an equipment using EIA 422-A drivers and receivers on the other side of the interface, if the leads of the receivers and drivers are properly configured to accommodate such an arrangement. For example, when using the MMJ scheme with the 6-conductor terminal interconnect cable, if there is an active control receiver on pin 6, it must be high impedance because it is sharing a common return on pin 4 with the data receiver and must be failsafed to -2 volts. The pin 6 receiver must be program disabled for these applications. Interconnection cable lengths are limited to the performance of the DEC423 side of the interface. When interconnecting with DEC423, remove the optional termination resistance from the EIA 422-A/V.11 receiver.

EIA 422-A drivers are not risetime controlled. Therefore, shielding may be required when interconnected with DEC423.

C.2.3 DEC423 INTERCONNECTION WITH EIA 232-D/V.28

Where DEC423 is interconnected with EIA 232-D/V.28, the data signaling rate limitations of EIA 232-D/V.28 shall apply. These limitations are discussed above for Curve D in Figure 17. Several types of "passive adapters" have been developed to facilitate interconnection of DEC423 using MMJ connectors to devices using the D Subminiature style connectors of EIA 232-D. Passive adapters and the DEC423 Active Converter (H3105) are described in Appendix D. The H3105 converts the EIA 232-D interface of a terminal into a DEC423 interface, providing DEC423 speed/distance performance and protection against ESD/EOS transients.

Figure 17: Data Rate Versus Cable Length for DEC423



C.2.4 How Far - How Fast

In any wired data transmission system, the two questions asked by users and sales people are; how far can I run the wires and how fast can I run the data? In every case of the how far-how fast query, the answer begins with "It depends." It depends on the factors referenced in this appendix. The numbers stated in Table 7 are those which can be guaranteed when used with the given conditions.

Table 7: Recommended DEC422 Drivers

Speed	Distance meters/feet	Comments
DEC 423		
9.6	900/3000	Using BC16H/J cable or theg standard 4 pair cable.
19.2*	300/1000	
38.4*	85/280	
EIA 423/V.10		
4.8	500/1600	
9.6	280/900	Using BC16H/J or the standard 4 pair cable.
19.2*	150/500	
38.4*	85/280	
EIA 232-D/V.28**		
9.6	15/50	Cable plus receiver must not exceed 2500 pF.
19.2*	15/50	
DEC423 to EIA 232-D**		
9.6	60/200	
19.2*	30/100	
38.4*	15/50	Note: EIA 232 does not cover above 20 kbps, this will work but do not call it EIA 232.

NOTE

*** Some Asyncronous devices (such as the DZ family, DMF and the like) have "Baud Rate Generator" errors, for example 19.8k bps. This, with line distortion, causes intermittent errors.**

NOTE

**** The upcoming EIA/TIA 562 permits higher speed operations, however; 1. The cable length and capacitance is considerably reduced, typically from 2500 pF to 800 pF. 2. The drive may be reduced to about 4 volts. Our protection devices and filter pins may add 1000 pF of capacitance. This message is to indicate that trouble free inter-operations may not be possible with the new standards. Every driver has its limit!**

APPENDIX D DEC423/EIA 232-D ADAPTERS

D.1 PASSIVE ADAPTERS

To bridge between old and new products, the H8571-X series of passive adapters have been developed to mate MMJ devices with those that use the EIA 25-pin D-subminiature connectors associated with the EIA 232-D standard. The H8571 adapters are used to adapt 25-pin and 9-pin Dsub connections to modified modular jack (MMJ) connections. Several adapters are required because of changes in the sex of the Dsub connector, whether the connection is to a DTE or DCE type interface device, the need for filtering (where the BC16E-XX cable replaces a shielded cable), and variances in the use of the EIA 232-D signals and their pinouts. Each adapter provides a MMJ on one side and a male or female Dsub connector on the other side with jack screws or hex nuts as appropriate. The following adapter types are available:

a. H8571-A: MMJ to 25-pin, female, filtered Dsub connector with jack screws for mating to terminal communications ports.

b. H8571-B: MMJ to 9-pin, female, filtered Dsub connector with jack screws for mating to 9-pin printer ports.

c. H8571-C: MMJ to 25-pin, male, unfiltered Dsub connector with mounting hex nuts for converting from the MMJ ports of the VT300 series terminals to an EIA-232 connection with forced control leads.

d. H8571-D: MMJ to 25-pin, male, filtered Dsub connector with jack screws for connection to the printer port of Rainbow Personal Computers.

e. H8571-E: MMJ to 25-pin, male, filtered Dsub connector with jack screws for connection to LJ250 color printers.

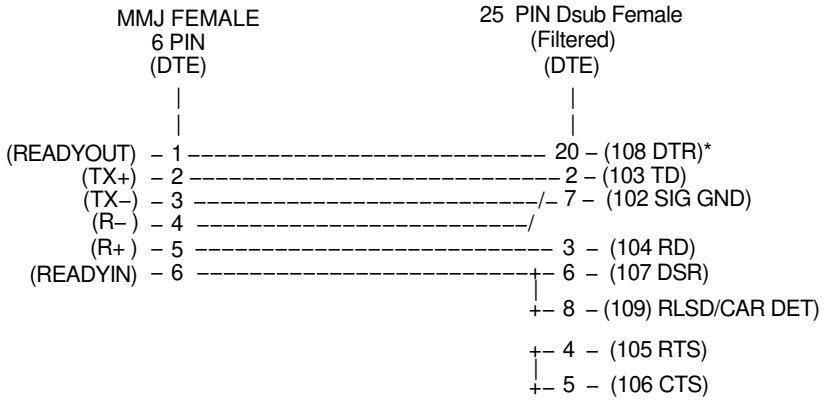
f. H8571-H: 12-23599-07 MMJ to 25-pin, female, filtered Dsub connector with jack screws for connection to VT320-A2, -B2, -C2 and the VT10A-AA, -AB terminals.

The wiring diagrams of these adapters and the reasons for their development are stated in the following subheads. Although in several cases these adapters were designed for specific products, they should meet the generic requirements of similar Digital products.

D.1.1 PASSIVE (25-PIN) ADAPTER (H8571-A)

The passive adapter (H8571-A) was the first adapter developed in the series to permit adaptation of the communication port or similar port (EIA 232-D, 25-pin Dsub, male) of a standard terminal (VT100 or VT200 series) to modified modular plug (MMP) terminated 6-conductor terminal interconnection cable (BC16E-XX). The H8571-A houses a 6-position female MMJ to a D Subminiature (Dsub) connector. For the H8571-A, a 25-pin, female, filtered Dsub connector with jack screws is specified and is wired as shown in Figure 18. A filter connector is required because the terminal communications port requires a shielded cable which is being replaced by unshielded BC16E-XX cable.

Figure 18: Passive Adapter (H8571-A) Wiring Detail

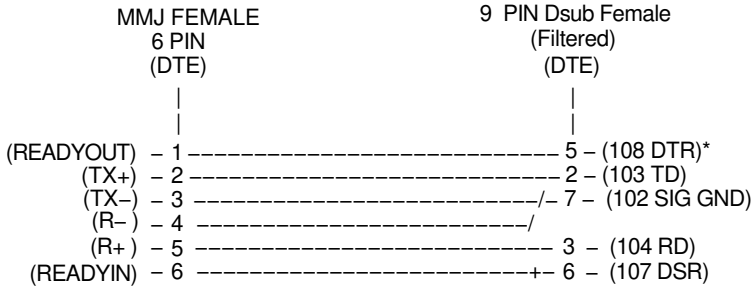

MMJ FEMALE
6 PIN
(DTE)
25 PIN Dsub Female
(Filtered)
(DTE)
(READYOUT) – 1 – 20 – (108 DTR)*
(TX+) – 2 – 2 – (103 TD)
(TX–) – 3 – 7 – (102 SIG GND)
(R–) – 4
(R+) – 5 – 3 – (104 RD)
(READYIN) – 6 – 6 – (107 DSR)
8 – (109) RLSD/CAR DET)
4 – (105 RTS)
5 – (106 CTS)

*Note: CCITT Circuit Number and Abbreviated Names

D.1.2 PASSIVE PRINTER PORT (9-PIN) ADAPTER (H8571-B)

The printer port adapter (H8571-B) was developed to permit adaptation of the VT200 series terminals (and similar products with the 9-pin Dsub printer port) to BC16E-XX cable. The H8571-B houses a 6-position female LAN connector to 9-pin, female, filtered Dsub connector with jack screws and is wired as shown in Figure 19. A filter connector is required because the printer port requires a shielded cable which is being replaced by unshielded BC16E-XX cable.

Figure 19: Passive Printer Port Adapter (H8571-B) Wiring Detail


MMJ FEMALE
6 PIN
(DTE)
9 PIN Dsub Female
(Filtered)
(DTE)
(READYOUT) – 1 – 5 – (108 DTR)*
(TX+) – 2 – 2 – (103 TD)
(TX–) – 3 – 7 – (102 SIG GND)
(R–) – 4
(R+) – 5 – 3 – (104 RD)
(READYIN) – 6 – 6 – (107 DSR)

*Note: CCITT Circuit Number and Abbreviated Names

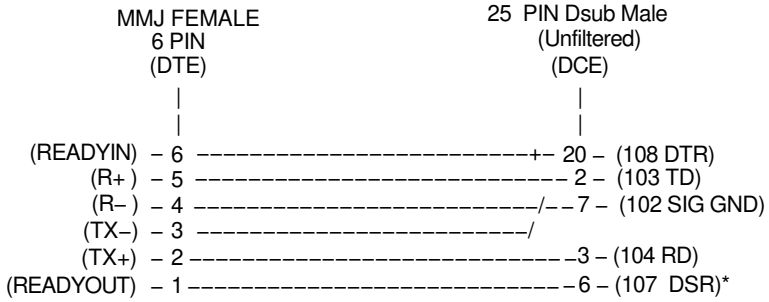
D.1.3 VT300 ADAPTER (H8571-C)

The VT300 was the first terminal to incorporate the DEC423 MMJ connector for direct BC16E-XX cable connection. The VT300 series has an optional EIA 232 25-pin Dsub port, two MMJ connector ports, and an MMJ printer port. For communications, customers may connect via the EIA 232 port or an MMJ. VT300 customers who wish to connect VT300 products into their existing EIA 232 wiring but have used the EIA 232 port on their VT300 for another connection will require the H8571-C to connect from an MMJ connector to an existing EIA 232 female cable connector.

The H8571-C combines a female MMJ connector with a 25-pin, male, unfiltered Dsub connector with mounting hex nuts to be compatible with the EIA 232 25-pin female terminated cable in existing wiring environments. A filter connector is not required because the DEC423 MMJ port has the required filtering designed into it so that it can be used with unshielded BC16E-XX cable.

Figure 20 contains a wiring diagram of the H8571-C showing the interconnection of the 6 position female MMJ connector to the Dsub connector.

Figure 20: VT300 Adapter (8571-C) Wiring Detail


MMJ FEMALE
6 PIN
(DTE)
25 PIN Dsub Male
(Unfiltered)
(DCE)
(READYIN) – 6 – 20 – (108 DTR)
(R+) – 5 – 2 – (103 TD)
(R–) – 4 – 7 – (102 SIG GND)
(TX–) – 3 –
(TX+) – 2 – 3 – (104 RD)
(READYOUT) – 1 – 6 – (107 DSR)*

*Note: CCITT Circuit Number and Abbreviated Names

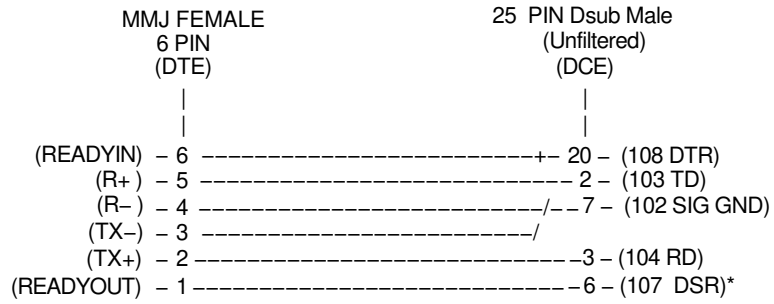
Note

A cost reduced version of this adapter was produced in the Far East. It is wired the same as the H8571-C. It is included with the purchase of a VT300 series terminal and cannot be purchased separately. Therefore, it does not have a part number.

D.1.4 RAINBOW ADAPTER (H8571-D)

The Rainbow adapter is required to connect the 25-pin, female Dsub printer port of the Rainbow to a BC16E-XX cable. The Rainbow adapter is identical to the VT300 Adapter (H8571-C) except that it uses a 25-pin, male, filtered Dsub connector and provides screws instead of nuts for fasteners. A filter connector is required because the printer port of the Rainbow requires a shielded cable which is being replaced by unshielded BC16E-XX cable. The internal connections are the same as for the H8571-C but are shown again in Figure 21 for completeness.

Figure 21: Rainbow Adapter (H8571-D) Wiring Detail

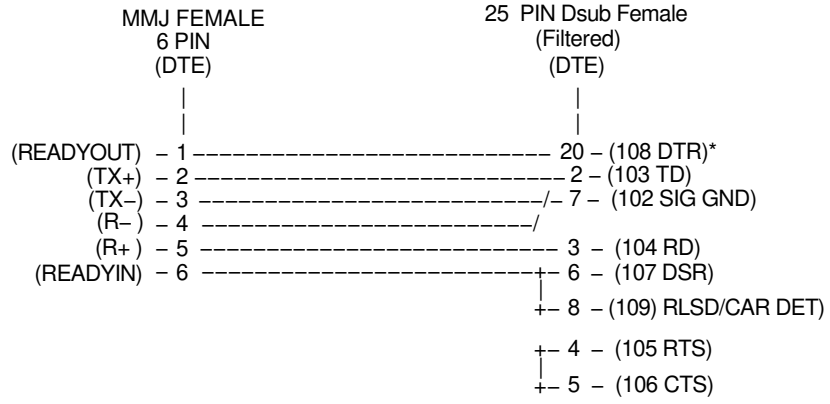

MMJ FEMALE
6 PIN
(DTE)
25 PIN Dsub Male
(Unfiltered)
(DCE)
(READYIN) – 6 – 20 – (108 DTR)
(R+) – 5 – 2 – (103 TD)
(R–) – 4 – 7 – (102 SIG GND)
(TX–) – 3 –
(TX+) – 2 – 3 – (104 RD)
(READYOUT) – 1 – 6 – (107 DSR)*

*Note: CCITT Circuit Number and Abbreviated Names

D.1.5 LJ250 ADAPTER (H8571-E)

The H8571-E is required because the LJ250 serial interface uses a female connector instead of a male connector typically provided with Digital printer devices. The sex reversal requires an adapter with a corresponding reversal of the MMJ pinouts. The H8571-E is similar to the Rainbow adapter (H8571-D) except that the MMJ pinouts are reversed as shown in Figure 22. The H8571-E connects a female MMJ connector to a 25-pin, male, filtered Dsub connector with jack screws.

Figure 22: LJ250 Adapter (H8571-E) Wiring Detail


MMJ FEMALE
6 PIN
(DTE)
25 PIN Dsub Female
(Filtered)
(DTE)
(READYOUT) – 1 – 20 – (108 DTR)*
(TX+) – 2 – 2 – (103 TD)
(TX–) – 3 – 7 – (102 SIG GND)
(R–) – 4 –
(R+) – 5 – 3 – (104 RD)
(READYIN) – 6 – 6 – (107 DSR)
8 – (109) RLSD/CAR DET)
4 – (105 RTS)
5 – (106 CTS)

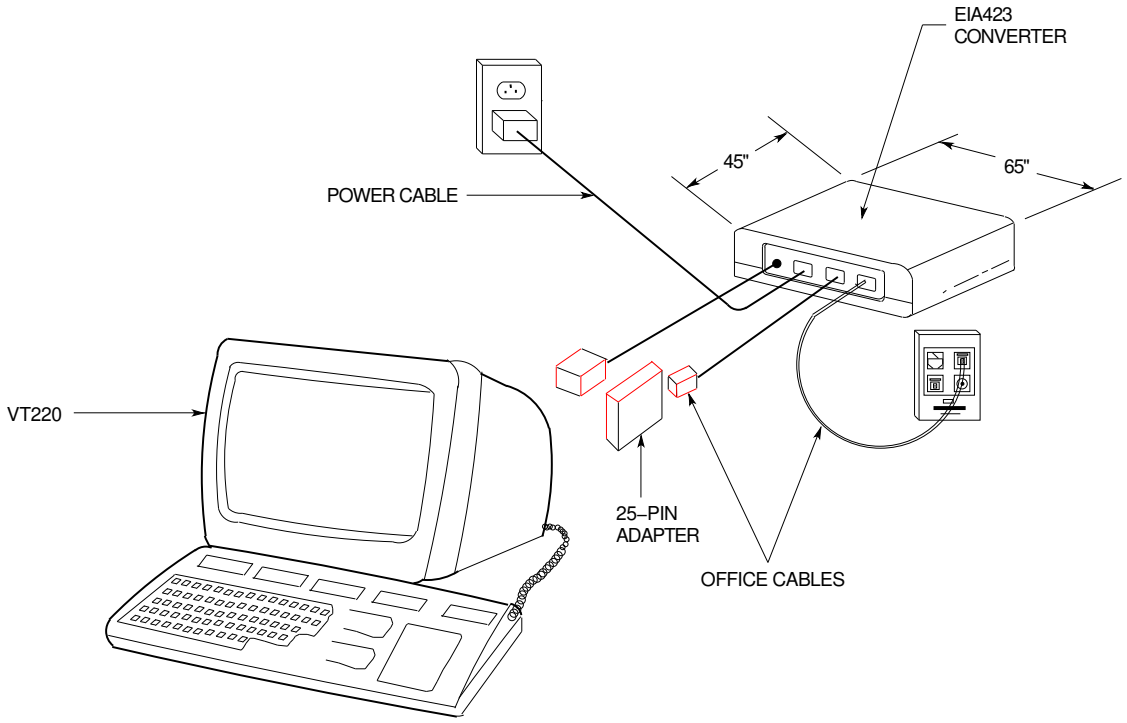
*Note: CCITT Circuit Number and Abbreviated Names

D.2 THE DEC423 ACTIVE CONVERTER

The DEC423 Active Converter (H3105) adapts the current generation of EIA 232 terminals to DEC423. Figure 23 illustrates the configuration of the DEC423 active converter with a VT220 terminal. A passive adapter and terminal interconnect cable (BC16E-XX) connect the terminal to the converter. A similar cable extends from the converter to a wall plate for

connection to a host system. The converter transforms EIA 232 signals into DEC423 signals and provides EOS/ESD protection for itself and the attached terminal. By transforming into DEC423 signals, terminal-to-host connections can be greatly increased without sacrificing performance. Terminals using the converter can attain the speed/distance performance shown in Appendix C for DEC423.

Figure 23: DEC 423 Active Converter with a VT220 Terminal



A block diagram of the DEC423 converter is shown in Figure 24. Power is fed through the converter to the terminal while an internal power supply powers the converter. This insures a common reference between the converter and terminal that will mitigate the effects of EOS/ESD transients. The converter uses DEC423 drivers and receivers which are protected on either side by transient suppressers and inductors as recommended in Appendix B. CCITT 108, Data Terminal Ready (DTR), is required to turn on the power to the converter drivers. Thus if the terminal is turned off, but the converter is not, the line to the host will appear to be disconnected.

Figure 24: DEC423 Converter (H-3105) Block Diagram

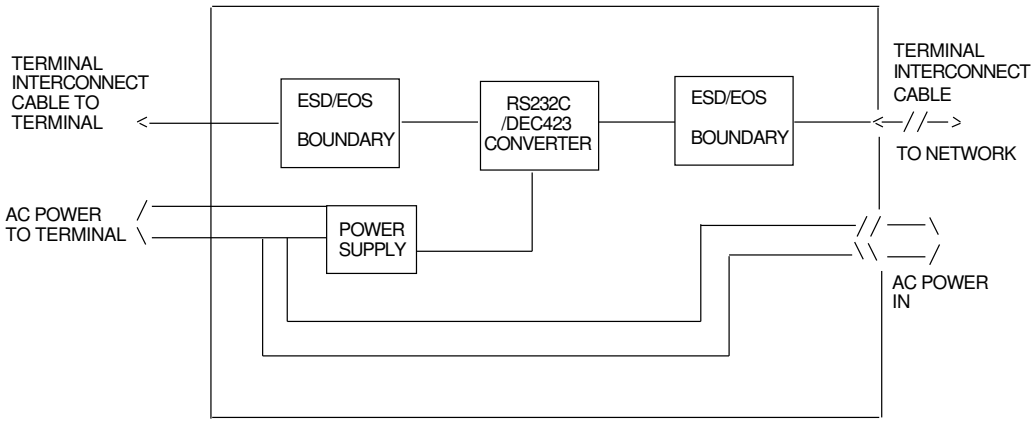


Figure 25shows the conversion of the EIA 232-D data line signals from the terminal to TTL levels and then to DEC423 levels at the network interface. The network driver disabling circuitry is shown also.

Figure 25: DEC423 Conversion Circuitry